

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)**

**CLASS: MTECH
BRANCH: ECE**

**SEMESTER : II
SESSION : SP/2025**

SUBJECT: EC596 FPGA & SYSTEM ON CHIP DESIGN

TIME: 3 Hours

FULL MARKS: 50

INSTRUCTIONS:

1. The question paper contains 5 questions each of 10 marks and total 50 marks.
 2. Attempt all questions.
 3. The missing data, if any, may be assumed suitably.
 4. Before attempting the question paper, be sure that you have got the correct question paper.
 5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.
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		CO	BL
Q.1(a)	Explain the VHDL orientation and applications and define the entity with suitable examples.	[5] 1	1
Q.1(b)	Design the 1 bit full adder circuit and write the Verilog@HDL code for the same.	[5] 1	1
Q.2(a)	Define the FPGA and design the important component on FPGA and explain with suitable circuit.	[5] 2	2
Q.2(b)	Explain the data types, file types, resolution functions with suitable examples.	[5] 2	2
Q.3(a)	Explain the synchronous and asynchronous counter. Design the 4 bit up and down counter.	[5] 2	2
Q.3(b)	Design the Modulo 5- counter and write the Verilog code for the system.	[5] 3	3
Q.4(a)	Define package, subpackage. Design the 4 bit shift register and write the Verilog@HDL code for the same.	[5] 3	3
Q.4(b)	Define the finite state machine with suitable examples.	[5] 4	3
Q.5(a)	Design the Layout of CMOS NAND-2 Gate and write the switching action of transistors.	[5] 5	4
Q.5(b)	Explore the IC Testing techniques. Show the IC techniques with suitable examples.	[5] 5	4

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