BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION SP/2025

CLASS: M.TECH **SEMESTER: II**
BRANCH: ECE **SESSION: SP-2025**

SUBJECT: EC583 DIGITAL VLSI DESIGN

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Realize the Boolean function Z = $\overline{AB + C(D + E)}$ using Dynamic CMOS Logic Style.	[5]	1	2, 3
Q.1(b)	Diagram a transistor-level circuit of 4-input NAND gate using Dynamic CMOS logic style	[5]	1	2, 3
Q.2(a)	Sketch transistor-level realization of a clocked D flip-flop from clocked SR flip-flop and explains its operation	[5]	2	2, 3
Q.2(b)	Show transistor-level implementation of SR flip-flop with NOR gate.	[5]	2	2
Q.3(a)	Sketch a cross-sectional view of a CMOS inverter in an n-well CMOS process.	[5]	3	3
Q.3(b)	Sketch a layout of 2-input NOR gate that has less drain area connected to the output and explain how this layout improves gate performance.	[5]	3	3
Q.4(a)	Schematize the transistor-level circuit diagram of Co (carry out) function Co= ABC_i(A+B), where Ci is the input carry to a 1-bit full adder.	[5]	4	6
Q.4(b)	Schematize the transistor-level circuit diagram of 1-bit full adder cell using transmission gate (TG) topology with minimum number of transistors.	[5]	4	6
Q.5(a)	Design a 6T SRAM cell and briefly explain its design requirements.	[5]	5	6
Q.5(b)	Schematize operation modes of 6T RAM cell assuming that left storage none storing a “0” and right storage node storing a “1”. Briefly explain its various operation modes.	[5]	5	6

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