BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATIONSP/2025)

CLASS: BTECH **SEMESTER : IV**
BRANCH: CSE/EEE **SESSION : SP/2025**

SUBJECT: EC261 DIGITAL COMPUTER ELECTRONICS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Consider a 3-bit binary number X_3 X_2 X_1 where X_1 is LSB. Design a circuit using NAND gate that will determine whenever the binary is greater than 3.	[2]	1	4
Q.1(b)	Design a Full subtractor circuit with a decoder and logic gate.	[3]	1	2
Q.2(a)	Develop a 4:2 priority encoder which has highest priority for highest order input	[2]	1	4
Q.2(b)	Design and describe BCD Adder circuit with suitable examples.	[3]	1	3
Q.3(a)	Realize BCD to seven segment decoder.	[2]	1	4
Q.3(b)	What is race-around condition in flip flop? Distinguish between Level triggering and edge triggering.	[3]	2	3
Q.4(a)	Explain with circuit diagram the working principle of a 4- bit SISO shift register.	[2]	2	1
Q.4(b)	Construct the excitation table for J-k and D flip flop. Using the excitation table Convert a J-K flip flop into a D flip flop.	[3]	2	1
Q.5(a)	Distinguish between synchronous and Asynchronous counter.	[2]	2	3
Q.5(b)	Design and describe 4-bit twisted ring counter with suitable example.	[3]	2	1

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