BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BCA **SEMESTER : II**
BRANCH: BCA **SESSION : SP/2025**

SUBJECT: CN123 BASICS OF DIGITAL COMPUTER AND LOGIC DESIGN

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Explain the working of a digital computer with block diagram. Represent the decimal number 6,248 in (a) BCD, (b) excess-3 code, (c) 2421 code, and (d) 6311 code.	[5]	1	1,2
Q.1(b)	Explain Complements. Perform subtraction on the given unsigned binary numbers using the 2's complement. (a) 10011 - 10010 (b) 100010 - 100110	[5]	1,2	2
Q.2(a)	Explain K-map. Simplifying the following Boolean function using three variable k- map. (i) xy + x'y'z' + x'yz' (ii) A'B + BC' + B'C'	[5]	3	3
Q.2(b)	Draw AND-OR gates implementation of the following function after simplifying it in (i) Sum of product (ii) Product of sum $F(A, B, C, D) = \sum(0, 2, 5, 6, 7, 8, 10)$	[5]	3	3
Q.3(a)	Define combinational circuit. Design a combinational circuit of three inputs and one output. The output is equal to 1, if the input variable have more 1's than 0's. The output is 0 otherwise.	[5]	3,4	4
Q.3(b)	Define a Decoder. Design a 4-bit adder cum subtractor circuit using full adder.	[5]	4	4
Q.4(a)	Design a sequential circuit with D flip-flops, A and B and one input x. When input x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transition from 00 to 01, 01 to 10, 10 to 11, 11 to 00 and repeats.	[5]	5	4,5
Q.4(b)	What is a register? Explain different types of registers. Illustrate the working of a 4-bit shift register with a suitable diagram.	[5]	4	2,4
Q.5(a)	Explain different classification of ROM and RAM.	[5]	3	2
Q.5(b)	Define Programmable Logic Devices. Differentiate between Programmable Logic Array (PLA) and Programmable Array Logic.	[5]	3	2

::::::26/04/2025::::::E