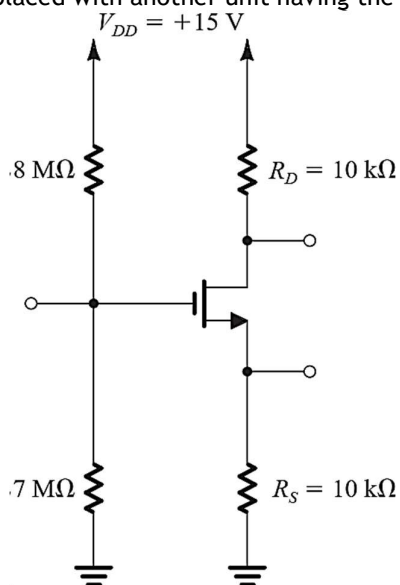


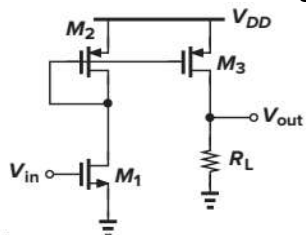
INSTRUCTIONS:

1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

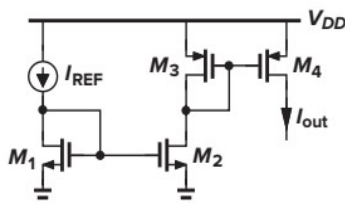
- Q.1(a) Determine the voltage gain for a CS Stage with Source Degeneration. [5]
 Q.1(b) It is required to design the circuit of Figure to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and for simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same but $V_t = 1.5$ V. [5]



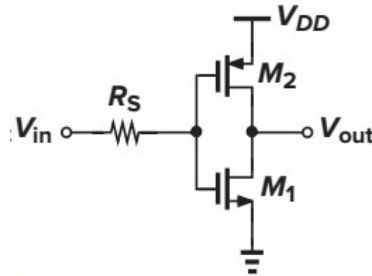
- Q.2(a) Calculate the small-signal voltage gain of the circuit shown in figure. [5]



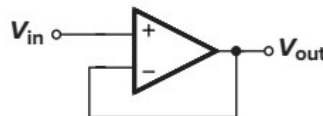
- Q.2(b) Determine the drain current of M4 if all of the transistors are in saturation and W/L ratio is different for every transistor. [5]



- Q.3(a) Determine the voltage gain of a Common Gate amplifier for high frequency application. [5]
 Q.3(b) Determine the transfer function of the complementary CS stage shown in figure. [5]



- Q.4(a) Find out common-mode to differential-mode conversion (A_{CM-DM}) due to g_m mismatch for differential amplifier. [5]
 Q.4(b) Determine $(V_{out1} - V_{out2})$ as a function of $(V_{in1} - V_{in2})$ for MOS differential pairs. [5]
 Q.5(a) Draw and explain differential input-output characteristics of a MOS differential pair. [5]
 Q.5(b) Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer depicted in figure. [5]



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