BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION SP/2023

CLASS: M.TECH/PRE-PHD **SEMESTER: II**
BRANCH: ECE **SESSION: SP-2023**

SUBJECT: EC583 DIGITAL VLSI DESIGN

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

		Marks	CO	BL
Q.1(a)	Describe switching threshold (V_M) of a CMOS inverter. Explain how its value is obtained graphically. What is the desired value of V_M for a CMOS inverter in 0.25 µm process.	[5]	1	1, 3
Q.1(b)	Consider a CMOS inverter circuit with the following parameters: V_{DD} = 3.3V, V_{tn} = 0.6V, V_{tp} = -0.7V, $ß_n$ = 200µA/V^2, $ß_p$ = 80 µA/V^2, Calculate the noise margins of the circuit.	[5]	1	4
Q.2(a)	Schematize transistor-level circuit of CMOS positive-level-sensitive D latch with minimum number MOSFET. Schematize transistor-level circuit of CMOS positive-edge-triggered D flip-flop.	[5]	2	6
Q.2(b)	Show transistor-level implementation of SR flip-flop with NOR gate.	[5]	2	2
Q.3(a)	What are the various basic CMOS technologies? Sketch the layout of CMOS NOT gate.	[5]	3	3
Q.3(b)	Sketch a transistor-level schematic of a 4-input domino AND gate and draw its optimized layout to improve its performance.	[5]	3	3
Q.4(a)	Schematize the implementation of the function sum = a XOR b XOR c in domino logic. Assume that the literals a, b, c and their complements are available as stable inputs to the gates. Two intermediate signals propagate (pi) and generate (Gi) are dynamically generated using XOR and AND gates.	[5]	4	6
Q.4(b)	Schematize the transistor-level circuit diagram of Co (carry out) function Co= ABC_i(A+B), S (sum) function S =ABC_i+($A + B + C_i)\overline{C_o}$, where Ci is the input carry to a 1-bit full adder.	[5]	4	6
Q.5(a)	Schematize 1T DRAM cell? Briefly explain its read, write and hold operations.	[5]	5	6
Q.5(b)	Design 6T SRAM cell and schematize its read operation model along with precharge circuit and sense amp circuit.	[5]	5	6

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