BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: M.TECH. **SEMESTER : II**
BRANCH: ECE **SESSION : SP/2023**

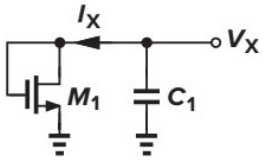
SUBJECT: EC581 ANALOG VLSI DESIGN

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

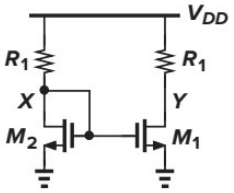
Q.1(a) Determine the voltage gain for a MOS source follower. [5]

Q.1(b) Find the V_x and I_X for the given circuit. [5]
And sketch V_X and I_X as a function of time.
Carrier mobility = μ_n, Oxide capacitance = C_{ox}, Width of the MOSFET = W, Length of the MOSFET = L, Threshold voltage = V_{th}



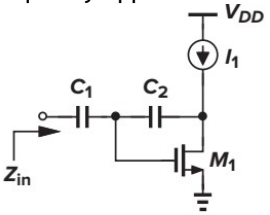
Q.2(a) What is the current mirror & what are its applications? [5]
What do you mean by Current Sink and Sources?

Q.2(b) Sketch V_X and V_Y as a function of time for the given circuit. [5]
Assume the transistors in each circuit are identical.



Q.3(a) Determine the voltage gain of a Common source amplifier for high frequency application. [5]

Q.3(b) Neglecting other capacitances, calculate the input impedance of each circuit shown in Figure. [5]



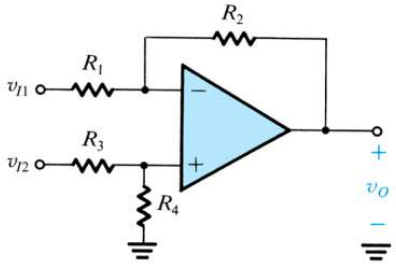
$\lambda = 0$

Q.4(a) Determine ($V_{out1} - V_{out2}$) as a function of ($V_{in1} - V_{in2}$) for MOS differential pairs. [5]

Q.4(b) Determine the Common-mode response for MOS differential pairs in the presence of resistor mismatch. [5]

Q.5(a) What do you mean by Slew Rate, and CMRR? [5]
Draw the building block of Voltage Operational Amplifier?

Q.5(b) Determine the output voltage of the following circuit. [5]



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