

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION SP/2023)**

CLASS: B.Tech.
BRANCH: ECE

SEMESTER : VI
SESSION : SP/2023

SUBJECT: EC365N MICROELECTRONIC DEVICES AND CIRCUITS

TIME: 02 Hours

FULL MARKS: 25

INSTRUCTIONS:

1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates

		CO	BL
Q.1(a) Outline the basic CMOS processes.	[2]	1	1
Q.1(b) Sketch a cross-section of a CMOS inverter in an n-well CMOS process.	[3]	2	3
Q.2(a) Outline the breakdown processes in reverse-biased diodes. Write the requirements of avalanche breakdown.	[2]	1	1
Q.2(b) Explain Band-to-Band Tunneling in a Reverse-Biased Diodes with suitable diagram. What is an upper-bound estimate of the peak electric field?	[3]	2	3
Q.3(a) List High-Field Effects in Gate Oxide.	[2]	2	3
Q.3(b) Write expression of Fowler-Nordheim tunneling current density and mention each term in it.	[3]	2	3
Q.4(a) Write down the long channel nMOS current model in linear, saturation and cut-off regions.	[2]	3	3
Q.4(b) The source voltage, threshold voltage and gain factor are given. what is the highest voltage that can be applied to the drain while the device operates in saturation? Neglecting the channel length modulation effect (i.e., $\lambda = 0$), calculate the drain current of Fig. (a) for $V_D = -0.4$ V and drain current of Fig. (b) for $V_D = -5$ V.	[3]	3	4
<div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;"> <p>+1V</p> <p>$V_{tp} = -0.4V$</p> <p>$\beta_p = 100 \mu A/V^2$</p> <p>(a)</p> </div> <div style="text-align: center;"> <p>+5V</p> <p>$V_{tp} = -2V$</p> <p>$\beta_p = 100 \mu A/V^2$</p> <p>(b)</p> </div> </div>			
Q.5(a) Draw a schematic showing the definitions of and relationship among the various definitions of channel length.	[2]	3	4
Q.5(b) Modern CMOS chips integrate billions of transistors side by side on a semiconducting common silicon substrate. Explain how they are electrically isolated from each other. Substantiate your answer with suitable sketch.	[3]	2	3