BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI (MID SEMESTER EXAMINATION SP/2023)

CLASS: B.Tech. SEMESTER: VI BRANCH: ECE SESSION: SP/2023

SUBJECT: EC365N MICROELECTRONIC DEVICES AND CIRCUITS

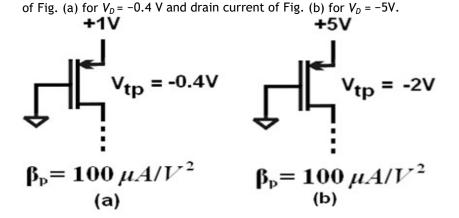
TIME: 02 Hours FULL MARKS: 25

INSTRUCTIONS:

- 1. The question paper contains 5 questions each of 5 marks and total 25 marks.
- 2. Attempt all questions.
- 3. The missing data, if any, may be assumed suitably.
- 4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates

Q.1(a) Q.1(b)	Outline the basic CMOS processes. Sketch a cross-section of a CMOS inverter in an n-well CMOS process.	[2] [3]	CO 1 2	BL 1 3
Q.2(a)	Outline the breakdown processes in reverse-biased diodes. Write the requirements of avalanche breakdown.	[2]	1	1
Q.2(b)	Explain Band-to-Band Tunneling in a Reverse-Biased Diodes with suitable diagram. What is an upper-bound estimate of the peak electric field?	[3]	2	3
Q.3(a) Q.3(b)	List High-Field Effects in Gate Oxide. Write expression of Fowler-Nordheim tunneling current density and mention each term in it.	[2] [3]	2 2	3
Q.4(a)	Write down the long channel nMOS current model in linear, saturation and cut-off regions.	[2]	3	3
Q.4(b)	The source voltage, threshold voltage and gain factor are given. what is the highest voltage that can be applied to the drain while the device operates in saturation?	[3]	3	4

Neglecting the channel length modulation effect (i.e., $\lambda = 0$), calculate the drain current



- Q.5(a) Draw a schematic showing the definitions of and relationship among the various [2] 3 4 definitions of channel length.
- Q.5(b) Modern CMOS chips integrate billions of transistors side by side on a semiconducting [3] 2 3 common silicon substrate. Explain how they are electrically isolated from each other. Substantiate your answer with suitable sketch.

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