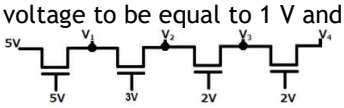
BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION SP/2023)

CLASS: B.TECH. **SEMESTER: VI**
BRANCH: ECE **SESSION: SP-2023**

SUBJECT: EC365N MICROELECTRONIC DEVICES AND CIRCUITS

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

		Marks	CO	BL
Q.1(a)	Descrite the important phenomena that occur in gate oxide layer due to high field across it? Explain the mechanism of GIDL with suitable diagram.	[5]	1	1, 2
Q.1(b)	Explain effect of high field on drift velocity of electron in silicon. Substantiate your answer with suitable diagram.	[5]	1	2
Q.2(a)	Estimate the voltages V_1, V_2, V_3, V_4 in the figure below given that the threshold voltage to be equal to 1 V and all these nodes have initially zero voltages. 	[5]	2	2
Q.2(b)	Write down the derivation steps of long channel nMOS current model in linear and saturation region.	[5]	2	3
Q.3(a)	Define transition frequency (f_t) and maximum oscillation frequency (f_{max}) of a MOS transistor.	[5]	3	1
Q.3(b)	Sketch a small-signal MOS transistor equivalent circuit with source (S) and body (B) at different potentials.	[5]	3	3
Q.4(a)	Explain the principles and characteristics of current mirror? Schematize a basic CMOS current mirror circuit and derive its current gain or current transfer ratio.	[5]	4	4,6
Q.4(b)	Explain the application of current mirror as current-steering circuit. Substantiate your answer with suitable diagram.	[5]	4	4
Q.5(a)	Schematize the layout of 2-input NAND gate that has less drain area connected to the output node and explain how this layout improves gate performance.	[5]	5	6
Q.5(b)	The major sources of errors in realizing capacitors are due to over etching (which causes the area to be smaller than the area of the layout masks) and an oxide-thickness gradient across the surface of the microcircuit. Schematize a simplified layout of a capacitor array to minimize these errors. Explain how the errors are minimized.	[5]	5	6

::::::02/05/2023::::::M