BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION SP/2023)

CLASS: BTECH **SEMESTER: IV**

BRANCH: MECH/CSE/EEE/IT **SESSION: SP/2023**

SUBJECT: EC261 DIGITAL COMPUTER ELECTRONICS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Implement a Full adder using NAND gate only.	[2]	CO1	BL4
Q.1(b)	Derive a logic expression that equal 1 only when the two binary numbers A_1A_0 and B_1B_0 have the same value. Draw the logic diagram and construct the truth table to verify the logic.	[3]	CO1	BL2
Q.2(a)	Realize a Full subtractor using a 3-line- to-8 line decoder.	[2]	CO1	BL4
Q.2(b)	Draw logic diagram of a BCD adder using two 4 bit adders and correction circuit.	[3]	CO1	BL3
Q.3(a)	Explain and draw logic diagram of BCD encoder.	[2]	CO1	BL4
Q.3(b)	Construct SR flip flop with NAND gates and obtain its characteristics equations.	[3]	CO2	BL3
Q.4(a)	Explain SISO shift register and PIPO shift register with diagram	[2]	CO2	BL1
Q.4(b)	Explain the operation of J-K flip flop. How does a J-K flip flop differ from an S-R flip flop in its operation?	[3]	CO2	BL1
Q.5(a)	Design a synchronous 3-bit Up counter Using J-K flip flops.	[2]	CO2	BL3
Q.5(b)	Explain the operation of 4-bit ring counter with diagram. Why is that name?	[3]	CO2	BL1

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