BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION SP2023)

CLASS: BTECH **SEMESTER: II**
BRANCH: BIOTECH/CIVIL/CHE/MECH/PROD **SESSION: SP/2023**

SUBJECT: EC101 BASICS OF ELECTRONICS AND COMMUNICATION ENGINEERING
TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

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Q.1(a)	Explain, how does a barrier field appear in an open circuited p-n junction diode. Sketch the electric field intensity, electrostatic potential curves as a function of distance across the junction.	[3]	1	2
Q.1(b)	A current flowing through a p-n junction Silicon diode is 60 mA for a forward bias voltage of 0.9 volt at room temperature 300 ^0K. Determine the static and dynamic resistances of the diode.	[2]	1	4
Q.2(a)	Explain the working principle of a Zener diode-based voltage regulator with a neat circuit diagram. Can we replace the Zener diode with a p-n junction diode in the regulator circuit? Justify your answer.	[3]	1	2
Q.2(b)	Find the range of input voltage to be applied to a Zener voltage regulator with a series resistance of 200 Ω to maintain a voltage of 30V across the load resistance of 2 KΩ. Assume the maximum power dissipated in the Zener diode is 750 mW.	[2]	1	4
Q.3(a)	Clearly explain the working principle of a center-tap full-wave diode rectifier with circuit diagram. Also, draw different voltage and current waveforms associated.	[3]	1	2
Q.3(b)	Derive expressions of rectification efficiency and voltage regulation for a center-tap full-wave diode rectifier.	[2]	1	4
Q.4(a)	Draw the circuit diagram for a transistor operating in common-emitter configuration. Explain its output characteristics, indicating the active, cut-off and saturation regions with characteristic diagram.	[3]	2	2
Q.4(b)	Derive the current relationship $I_C = \beta I_B + I_{CEO}$, where I_C and I_B are representing the collector and base currents of a transistor, β is the current gain and I_{CEO} is the reverse saturation current when base is open circuited.	[2]	2	4
Q.5(a)	Draw the circuit diagram for a fixed-bias considering an n-p-n transistor in CE-configuration mode of operation. Obtain expressions for its zero-signal operating point voltage and current values.	[3]	2	2
Q.5(b)	Design a fixed-bias circuit for a CE-transistor amplifier such that operating point is $V_{CE} = 8V$ and $I_C = 2\ mA$. The circuit is supplied with a fixed 15 V dc-supply and a silicon transistor with $\beta = 100$.	[2]	2	4

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