BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI (END SEMESTER EXAMINATION)

CLASS: M. Tech SEMESTER : 2 nd BRANCH: EEE SESSION : SP/22 SUBJECT: EE561 Embedded Control of Switching Power Converter TIME: 2Hrs FULL MARKS: 50		
INSTRUCTION 1. The que 2. Attempt 3. The miss 4. Before a 5. Tables/D	DNS: stion paper contains 5 questions each of 10 marks and total 50 marks. all questions. sing data, if any, may be assumed suitably. Ittempting the question paper, be sure that you have got the correct question paper. Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.	
Q.1(a)	Differentiate between linear power supply and switched mode power supply (SMPS) based upon	[5]
Q.1(b) CO1	List two application of SMPS in renewable energy harnessing.	[5]
Q.2(a) CO2	Obtain small signal model of a Boost converter.	[5]
Q.2(b) CO2	Obtain transfer functions relationship between small signal change in output voltage $(\hat{V}_{\mathcal{C}})$ and small signal change input duty cycle (\hat{d}) in case of Boost Converter.	[5]
Q.3(a) CO3	Obtain transfer functions relationship between small signal change in inductor current (\hat{i}_L) signal change input duty cycle (\widehat{d}) in case of Buck Converter.	[5]
Q.3(b) CO3	Obtain transfer functions relationship between small signal change in inductor current (\hat{t}_L) signal change input voltage (\hat{V}_a) in case of Buck Converter.	[5]
Q.4(a) CO4	Obtain input output current relationship of a Buck converter with at least one series non- ideality.	[5]
Q.4(b) CO4	Compare input-output relationship of current of non-ideal buck converter and ideal buck converter	[5]
Q.5(a) CO5	Write a program for ATMEGA2560 microcontroller to produce one pulse of 10kHz with 50% duty cycle in same phase using TIMER1.	[5]
0.5(h)	Design an embedded system block diagram for closed loop voltage control of DC-DC Buck	[5]

Q.5(b) Design an embedded system block diagram for closed loop voltage control of DC-DC Buck [5] CO5 converter

29/04/2022 E