BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: B.TECH. **SEMESTER: VI**
BRANCH: ECE **SESSION: SP/22**

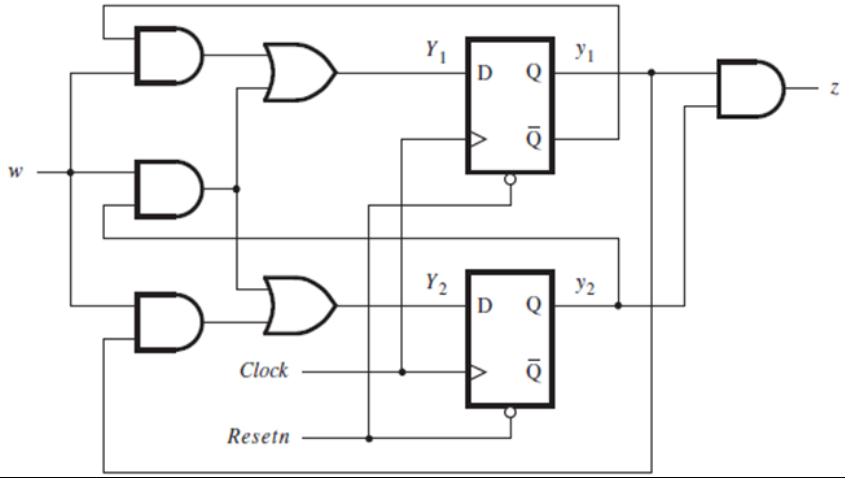
SUBJECT: EC361 Digital System Design with FPGAs

TIME: 2:00 Hrs **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 2 Sections: Section-A and Section-B.
2. Attempt all questions in Section-A with 30 MCQs each of 1 mark (total 30 marks) and all questions in Section-B with 5 questions each of 4 marks (total 20 marks).
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data handbook/Graph paper etc. to be supplied to the candidates in the examination hall.

Q. No.	Section-A (MCQ)	Answer
1.	The early ICs were designed using (a) standard cells (b) gate arrays (c) reconfigurable hardware (d) full custom design techniques.	
2.	The datapath is a block in a generic digital processor, which (a) performs all computations (b) determines what actions happen in the processor at any given point in time (c) stores all computational results for future use (d) interconnects various blocks of the processor.	
3.	(Tick on the wrong answer). Few design-automation tools which are indispensable in the custom-design process are (a) layout editors, (b) design-rule and electrical-rule checkers, (c) parasitics extractor, (d) routers.	
4.	The most important goal of the standard-cell placement and routing tools is to minimize the interconnect length, which is achieved by using (a) feed-back cell (b) feed-forward cell (c) feed-through cell (d) none of these.	
5.	With seven or more metal levels and three-dimensional approach, the standard-cell design achieves more than (a) 50% density (b) 60% density (c) 70% density (d) 90% density.	
6.	The sea-of-gates implemented in a 0.6-μm CMOS technology has a maximum capacity of (a) 100 K gates (b) 200 K gates (c) 300 K gates (d) 400 K gates.	
7.	Clock jitter is the result of clock signal's (a) temporal variation (b) spatial variation (c) process variation (d) temperature.	
8.	Tick on wrong answer.) (a) Clock skew is caused by static path-length mismatches, (b) Clock skew is constant from cycle to cycle, (c) Clock skew results in clock period variation, (d) Clock skew results in phase shift.	
9.	(Tick on wrong statement.) Routing the clock in the opposite direction of the data (a) avoids malfunctioning of circuit, (b) degrades the circuit performance, (c) results in positive skew, (d) results in negative skew.	
10.	Distributed buffers are integral components of the clock distribution networks, as they are required to drive (a) the register loads, (b) the global interconnects, (c) local interconnects, (d) all of them.	
11.	(Tick on wrong answer.) The critical dimension of polysilicon gate material is its width, variation of which causes variation in device (a) channel length, (b) drive current, (c) switching characteristics, (d) threshold voltage.	
12.	(Tick on wrong answer.) Major source of jitter is the variation in (a) power supply (b) circuit layout density, (c) polysilicon gate width, (d) temperature.	
13.	Total number of transistors required by mirror adder is (a) 18 (b) 20 (c) 22 (d) 24.	
14.	(Tick on wrong answer). The ripple adder is (a) faster for small values of N (b) Carry-bypass adder is faster for larger value of N (c) delay crossover point occurs for N between 4 and 8 bits (d) none of these.	
15.	For vector merging in pipelined multipliers the best choice is (a) Mirror adder (b) static CMOS adder (c) TG adder (d) carry-lookahead adder.	
16.	Which is not the design time dynamic power reduction technique? (a) Lower V_{DD}, (b) Multi-V_{DD} (c) Transistor sizing (d) Muti-Vt.	
17.	Which is the most attractive approach of power reduction technique? (a) (a) transistor sizing, (b) clock gating (c) dynamic voltage scaling (d) V_{DD} scaling.	
18.	With the use of Multi-Vt technology, we can trade off speed for (a) power, (b) area, (c) noise margin, (d) none of these.	
19.	Which of the caches are closer to the core of a processer? (a) Level 1, (b) Level 2, (c) Level 3, (d) None of them.	
20.	NOR ROM is nothing other than a (a) pseudo-NMOS NOR gate (b) pseudo-NMOS NAND gate (c) pseudo-NMOS NOT gate (d) pseudo-NMOS OR gate.	
21.	UV light erase mechanism is adopted in (a) EPROM (b) EEPROM (c) Flash EEPROM (d) mask	

	ROM.	
22.	(Tick on the wrong answer). Column circuitry required for each column is a (a) Bitline conditioner (b) Sense amplifier (c) Column multiplexer (d) Row decoder.	
23.	Bitline equalizer is a part of (a) bitline conditioning circuit (b) row decoder (c) column decoder (d) sense amplifier.	
24.	What kind of failures may occur in SRAM cell? (a) Hard failure, (b) Soft failure, (c) Parametric failure, (d) All of them.	
25.	Test which is subdivided into static (dc) and dynamic (ac) tests is (a) diagnostic test (b) functional test (c) parametric test (d) all of these.	
26.	Ad hoc test approach includes (a) partitioning of large state machines, (b) addition of extra test points, (c) provision of reset states, (d) all of these.	
27.	level-sensitive scan design (LSSD) was obligatory within (a) IBM, (b) Intel, (c) AMD, (d) NXP.	
28.	(Tick on wrong answer). Built-in Self-Test (BIST) contains (a) stimulus generator (b) response analyzer (c) Test controller (d) none of these.	
29.	Pseudo random sequence generator with characteristic polynomial $P(x) = 1 + x + x^4$ has (a) 2 Flops (b) 3 Flops (c) 4 Flops (d) 5 Flops.	
30.	(Tick on the wrong answer). What precautionary measure is to be taken for IDDQ testing? (a) pseudo-nMOS gates must be disabled (b) analog circuits must be disabled (c) Dynamic gates must be disabled (d) Static CMOS gates must be disabled.	

		Section-B	
CO2	Q.1(a)	Show a diagram to explain the role of switch matrix in FPGA, where more than one CLB is required to accommodate the intended design.	[2]
CO2	Q.1(b)	Briefly explain the main applications of FPGA.	[2]
CO1	Q.2(a)	What are the various sources of skew and jitter in synchronous clock distribution network?	[2]
CO2	Q.2(b)	Substantiate your answer with suitable diagram.	[2]
CO3	Q.3(a)	Show the static CMOS implementation of the Co (carry out) function.	[2]
CO3	Q.3(b)	What is the smart design trick that has been adopted in designing 1-bit static CMOS full adder?	[2]
CO5	Q.4(a)	Design a 1-bit embedded cache memory.	[2]
CO1	Q.4(b)	Define PR (pull-up ratio) or γ-ratio in relation to 6T SRAM cell. Define CR (cell ratio) or ß-ratio in relation to 6T SRAM cell.	[2]
CO5	Q.5(a)	A sequential circuit is given below for testing with scan-based technique. Draw a test setup circuit. 	[2]
CO4	Q.5(b)	Explain how to test the combinational part of the circuit with the drawn test setup and explain how to test the sequential part of the circuit with the same test setup and suitable test vector.	[2]