BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: IMSC **SEMESTER: VI**
BRANCH: MATHS & COMPUTING **SESSION : SP/2020**

SUBJECT : CS4109 COMPUTER SYSTEM ARCHITECTURE

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) How design procedure & performance of the computer changes with time? [2]
(b) Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps & a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps & a CPI of 1.2 for the same program. Which computer is faster for this program & by how much? [3]

Q2 (a) Why have been computer designed to use the binary number system? [2]
(b) Carry out the following conversions: [3]
$(1011011)_2 \rightarrow (\quad)_{10} \rightarrow (\quad)_8 \rightarrow (\quad)_{16}$

Q3 (a) Give behavioral description of a full adder. Also draw the truth table. [2]
(b) Define an encoder. Explain Octal to Binary Encoder. [3]

Q4 (a) What are the important elements of bus design? [2]
(b) What is an interrupt? How is it executed? Show the program flow with interrupts. [3]

Q5 (a) Differentiate between combinational and sequential circuits. [2]
(b) Perform $(11011)_2 - (10011)_2$ [3]

Q6 (a) Draw the flowchart for floating point addition of 2 numbers. [2]
(b) What decimal number is represented by this single precision float: [3]
11000000101000000000000000000000

:::::: 27/02/2020 ::::::M