BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE **SEMESTER: IV**
BRANCH: ECE **SESSION : SP/2019**

SUBJECT : EC4201 VLSI DESIGN

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) Explain the Orientation of VHDL & Verilog. [2]
(b) Define Y- chart with physical, behavioral and structural domain. [3]

Q2 (a) Explain the Structural architecture with suitable examples. [2]
(b) Derived the Expression for Drain Current of NMOS Transistor and draw the I_D-V_D Characteristics [3]
$I_D = \mu_n C_{ox}(W/L) [(V_{GS}-V_{Tn}) V_{DS}- V^2_{DS}/2]$

Q3 (a) Explain the CMOS n-well process. [2]
(b) Design 4bit fulladder using VHDL and Verilog with structural architecture technique. [3]

Q4 (a) Explain the difference between SOI and P-well process. [2]
(b) Define (i) EAROM & (ii) Thin film transistor [3]

Q5 (a) Describe the layer representation. [2]
(b) Build a 2-input CMOS OR gate using a minimum number of transistors. [3]

Q6 (a) Explain the latch up and latchup Triggering. [2]
(b) Design 2- input NAND gate using MOS logic & write the switching action of the transistors. [3]
Design the layout of 2-input NOR gate with showing the correct aspect ratio.

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