BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : IV**
BRANCH: ECE **SESSION : SP/19**

SUBJECT: EC4201 VLSI DESIGN

TIME: 3.00 Hrs. **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	Demonstrate the physical, behavioral and structural representation with Y- chart.	[2]
Q.1(b)	Explain the difference between Full Custom VLSI Design & Semi-custom VLSI Design.	[4]
Q.1(c)	Write the VHDL code for 4 bit Comparator.	[6]
Q.2(a)	Explain the CMOS fabrication process.	[2]
Q.2(b)	Explain the difference between SOI and N-well process.	[4]
Q.2(c)	Define (i) EAROM & (ii) latch up prevention techniques	[6]
Q.3(a)	Describe the Latch up triggering.	[2]
Q.3(b)	Build a 2-input NOR gate using a minimum number of CMOS transistors.	[4]
Q.3(c)	Explain the capacitance & resistance estimation. Show the process to design the layout of capacitor.	[6]
Q.4(a)	Explain the difference between FPGA & CPLD.	[2]
Q.4(b)	Design 3- input AND gate using MOS logic & write the switching action of the transistors.	[4]
Q.4(c)	Design the layout of 3-input NOR gate with showing the correct aspect ratio.	[6]
Q.5(a)	Draw & explain the Current Mirror Circuit.	[2]
Q.5(b)	Draw the layout of CMOS Inverter circuit and explain with equivalent fabrication monogram.	[4]
Q.5(c)	Draw the Circuit diagram of Operational Amplifier and explain CMRR, ICMR, PSRR, SR, and role of coupling capacitor.	[6]
Q.6(a)	Define Regularity & Modularity.	[2]
Q.6(b)	Demonstrate the circuit optimization techniques with suitable examples.	[4]
Q.6(c)	Explain the terms Placement, routing, hierarchy & Standard cell design.	[6]
Q.7(a)	Design Modulo 6 counters.	[2]
Q.7(b)	Design the half adder circuit using Transmission logic.	[4]
Q.7(c)	Demonstrate the types of memory with suitable examples and basic circuit diagram.	[6]

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