## BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI (MID SEMESTER EXAMINATION)

CL.	ASS:	IMSC	SEMESTER:VI/ADD
BR	ANCH	: MATHS & COMP.	SESSION : SP/2019
		SUBJECT : CS4109 COMPUTER SYSTEM ARCHITECTURE	
TIA	AE:	1.5 HOURS	FULL MARKS: 25
<ol> <li>INSTRUCTIONS:</li> <li>The total marks of the questions are 30.</li> <li>Candidates may attempt for all 30 marks.</li> <li>In those cases where the marks obtained exceed 25 marks, the excess will be ignored.</li> <li>Before attempting the question paper, be sure that you have got the correct question paper.</li> <li>The missing data, if any, may be assumed suitably.</li> </ol>			
Q1	(a)	Define the term computer system architecture.	[2]
	(b)	State the parameters which affect the performance of a computer.	[3]
Q2	(a) (b)	What are the different levels of system design? Give behavioural VHDL description of a half adder. Develop the truth tal same.	[2] ble for the [3]
Q3	(a)	Differentiate between RISC & CISC processors.	[2]
	(b)	Explain the functions of CPU & draw its functional flow chart.	[3]
Q4	(a)	Explain the basic instruction cycle with state transition diagram.	[2]
	(b)	Represent (-1.75) <sub>10</sub> in IEEE754 floating point format.	[3]
Q5	(a) (b)	<ul> <li>Explain the various instruction types &amp; formats.</li> <li>What are smallest and largest integers representable in 8-bit values usin <ul> <li>(i) Unsigned binary representation.</li> <li>(ii) Signed-magnitude binary representation.</li> <li>(iii) Two's complement representation.</li> </ul> </li> </ul>	[2] g [3]
Q6	(a)	How the data path is designed?	[2]
	(b)	Explain the working of Booth's Algorithm for 7*3.	[3]

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