BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE **SEMESTER: IV**
BRANCH: CSE **SESSION : SP/2019**

SUBJECT : CS4109 COMPUTER SYSTEM ARCHITECTURE

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1	(a)	Explain the difference between structure and behavior in the digital system design context.	[2]
	(b)	What is HDL? Write an HDL program for 8-bit binary multiplication.	[3]
Q2	(a)	What are the major component types at register level design?	[2]
	(b)	Explain the operation and design of 4-bit magnitude comparator.	[3]
Q3	(a)	Definite between CISC and RISC based computer system.	[2]
	(b)	What is PLDs? Sketch the ROM implementation of full adder.	[3]
Q4	(a)	Explain the single bit error detection and correction methods with diagram.	[2]
	(b)	How the fixed-point numbers represented in the computer system?	[3]
Q5	(a)	What is relative addressing? What are its advantages and disadvantages of this addressing mode?	[2]
	(b)	Discuss the queueing models considering single-queue and single-server and analyses its performance.	[3]
Q6	(a)	Draw and explain the structure of sequential arithmetic-logic unit (ALU).	[2]
	(b)	Explain the Booth's multiplication with the help of flow-chart and circuit by considering two numbers -9 and -13.	[3]

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