BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : IV**
BRANCH: CSE **SESSION : SP/19**

SUBJECT: CS4109 COMPUTER SYSTEM ARCHITECTURE

TIME: 3.00 Hrs. **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	Realize the full-adder with help of universal gates and not gates.	[2]
Q.1(b)	Explain the gate level and register level design process.	[4]
Q.1(c)	Implement the four-bit—stream serial adder stating its state table and truth table.	[6]
Q.2(a)	Differentiate between user mode and supervisor mode.	[2]
Q.2(b)	Explain M/ M/1 model of computer system.	[4]
Q.2(c)	How the floating-point numbers represented in the computer system?	[6]
Q.3(a)	What is Bus arbitration?	[2]
Q.3(b)	Explain the n-bit combinational arithmetic logic unit operation with suitable diagram.	[4]
Q.3(c)	Consider (-7) and (-5) for Booth's multiplication. Draw flowchart and required circuitry for Booth's multiplication.	[6]
Q.4(a)	What is an instruction pipeline?	[2]
Q.4(b)	Differentiate Microprogrammed control from hardwired control.	[4]
Q.4(c)	What is hardwired control and micro-programmed control? Explain the state table method and delay element method for hardwired design.	[6]
Q.5(a)	What is memory fragmentation?	[2]
Q.5(b)	Consider a paging system which uses the following page reference string with three-page frame capacity. Use the page replacement algorithm (FIFO, LRU and OPT), to sketch and find the page number of faults in each case. 2 3 2 1 5 2 4 5 3 2 5 2	[4]
Q.5(c)	A computer uses RAM chip of 1024X1 capacities. (i) How many chips are needed to provide a memory capacity of 16 bytes? (ii) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?	[6]
Q.6(a)	What is associative memory?	[2]
Q.6(b)	Explain the serial mode of transmission along with its different types.	[4]
Q.6(c)	Explain different data transfer techniques with diagram.	[6]
Q.7(a)	What is an instruction cycle?	[2]
Q.7(b)	Discuss the different types of hazards in context of pipeline processing.	[4]
Q.7(c)	Write short notes on parallel processing.	[6]

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