**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**
**(END SEMESTER EXAMINATION)**

**CLASS: IMSc** **SEMESTER : VI/ADD**
**BRANCH: MATHS AND COMPUTING** **SESSION : SP/19**

**SUBJECT CS4109 COMPUTER SYSTEM AND ARCHITECTURE**

**TIME: 3 Hours** **FULL MARKS: 60**

**INSTRUCTIONS:**
**1. The question paper contains 7 questions each of 12 marks and total 84 marks.**
**2. Candidates may attempt any 5 questions maximum of 60 marks.**
**3. The missing data, if any, may be assumed suitably.**
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
**5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.**

---

Q.1(a) How design procedure and performance of the computer changes with time. [2]

Q.1(b) Discuss the important features of RISC and CISC Architecture. [4]

Q.1(c) Consider two different hardware implementations $M_1$ & $M_2$ of the same instruction set. There are three classes F, I & N of instructions in the instruction set. $M_1$clock rate is 600 MHz, $M_2$'s clock cycle is 2ns. The average CPI for the three instruction classes on $M_1$ & $M_2$ are as follows: [6]

| Class | CPI for $M_1$ | CPI for $M_2$ | Comments |
|---|---|---|---|
| F | 5.0 | 4.0 | Floating Point |
| I | 2.0 | 3.8 | Integer Arithmetic |
| N | 2.4 | 2.0 | Non-arithmetic |

(a) What are the peak performances of $M_1$ & $M_2$ in MIPS?
(b) If 50% of all instructions executed in a certain program are form class N, and the rest are divided equally among F and I, which machine is faster and by what factor?
(c) Designers of $M_1$ plan to redesign the machine for better performance. With the assumptions of part (b), which of the following redesign options has the greatest performance impact and why?
1. Using a faster floating point unit with double the speed (Class F CPI = 2.5)
2. Adding a second integer ALU to reduce the integer CPI to 1.20
3. Using faster logic that allows a clock rate of 750MHz with the same CPIs.

Q.2(a) List Register level components. [2]

Q.2(b) Explain the different components of Processor level design. [4]

Q.2(c) Discuss the design of Full Adder with the circuit. Also Draw the truth table. [6]

Q.3(a) What are the Registers necessary to fetch, decode and execute an instructions? [2]

Q.3(b) Add the numbers $(0.75)_{10}$ and $(-0.275)_{10}$ in binary using the Floating-Point Addition Algorithm. [4]

Q.3(c) Multiply -7x3 using Booth's Algorithm. [6]

Q.4(a) List the functions of Control Unit. [2]

Q.4(b) Describe the hard wired control unit. [4]

Q.4(c) Define Addressing Mode. Explain the different types of Addressing Modes with an example. [6]

Q.5(a) Why one type of RAM is considered to be an Analog and the other Digital? [2]

Q.5(b) A block Set-Associative Cache consist of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consisting of 128 words. [4]

1. How many bits are there in the main memory address?
2. How many bits are there in each of the TAG, SET and word fields.
3. What is the size of the cache memory?

Q.5(c) What is Cache Coherence? Explain the different Cache Memory addressing mapping schemes? [6]

Q.6(a) Distinguish between Synchronous and Asynchronous Bus Operation. [2]

Q.6(b) Explain the following instructions: [4]

1. MOV r, M 2. ADC r 3. ANA r

Q.6(c) What is DMA? Why are the R/W control lines in a DMA Controller bidirectional? Explain. [6]

Q.7(a) List the major factors affecting the performance of a pipeline. [2]

Q.7(b) Explain the different pipeline hazards with example. [4]

Q.7(c) Write the zero and one address instruction for the following expression: [6]

X = A*(B-C)/E+F-G)

**:::::24/04/2019 E:::::**