BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII**
BRANCH: EEE **SESSION : MO/2025**

SUBJECT: EE573 EMBEDDED SYSTEMS AND APPLICATIONS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Draw a basic block diagram of an embedded system showing dataflow and control signals	[5]	1	1
Q.1(b)	List two different types of ROM, and explain their role in an embedded system.	[5]	1	1
Q.2(a)	Explain operating principle of SPI communication with an appropriate timing diagram.	[5]	2	2
Q.2(b)	Write an Embedded C code for writing the data 0x55H to memory address 0x01H of a slave with 0xA0H address using I2C communication.	[5]	2	2
Q.3(a)	Apply simultaneous execution of one arithmetic instruction and logical operation in one instruction cycle, using a suitable assembly code for TMS320C6713 . Both instructions should be executed in single instruction cycle	[5]	3	3
Q.3(b)	Apply simultaneous execution of (a) loading two new data in two data from A1 and B1 to A2 and B2 (2) Multiply the previously loaded data in A2 and B2 (3) store the previously multiplied result in A4. All these instructions should be executed in one single instruction cycle.	[5]	3	3
Q.4(a)	Analyze the role of TCCR0 for CTC wave generation mode.	[5]	4	4
Q.4(b)	Write a program to toggle an LED every 8ms, assuming the clock frequency of ATMEGA328 to be 16MHz using TIMER0.	[5]	4	4
Q.5(a)	Design a closed loop speed control of three phase induction motor using TMS320F28379D with the help of a proper block diagram showing data flow and control signal.	[5]	5	5
Q.5(b)	Design inter-interconnection of CLA, CLB, DMA, and CPU for the speed control operation.	[5]	5	5

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