BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: B. TECH. **SEMESTER : III/ADD**
BRANCH: EEE **SESSION : MO/2025**

SUBJECT: EE24203 ANALOG AND DIGITAL CIRCUITS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

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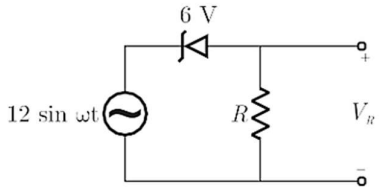
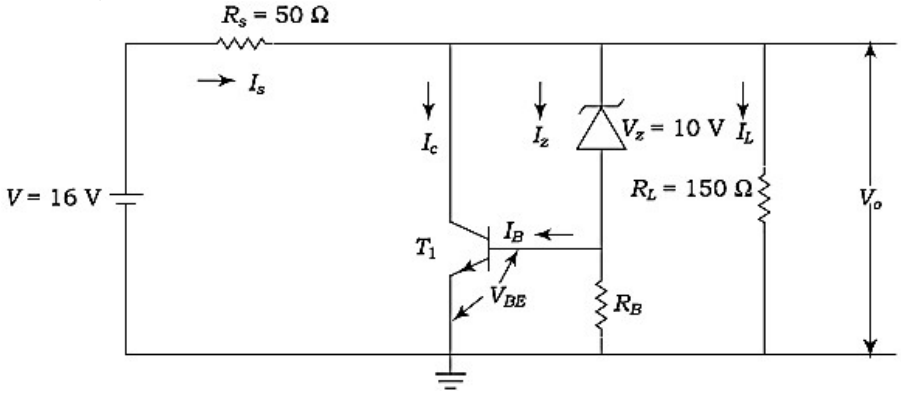
Q.1(a) For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 volts. Draw the waveform observed across R for sinusoidal input voltage. [5]

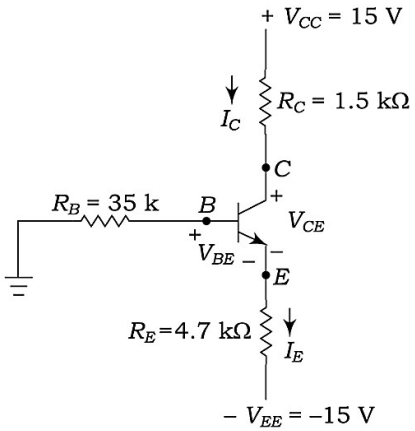


Write, with a suitable circuit diagram, the working principle of a positive clamper circuit.

Q.1(b) A transistor shunt regulated power supply is shown in Figure. Determine (a) the output voltage (V_O), (b) load current (I_L), and (c) source current (I_S). Assume zener resistance is equal to zero, V_{BE}= 0.7 V and R_B =∞. [5]



Q.2(a) Determine the emitter current, collector current, and collector to emitter voltage. Assume V_{BE} = 0.75 V and β = 70. [5]



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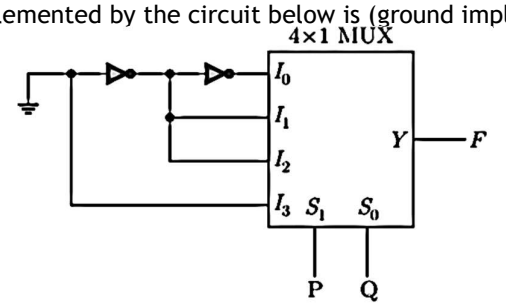
Q.2(b) Draw the high-frequency small-signal hybrid-π model of a voltage-divider-biased CE amplifier and its complete frequency-response curve. [5]
Illustrate the working of a Wien bridge oscillator with a neat circuit diagram.

Q.3(a) Determine the gain of a common-source amplifier with voltage-divider bias in the mid-band region. [5]

Q.3(b) Determine the radix r: $(BEE)_r = (2699)_{10}$ [5]
Draw and explain the working principal of CMOS Inverter.

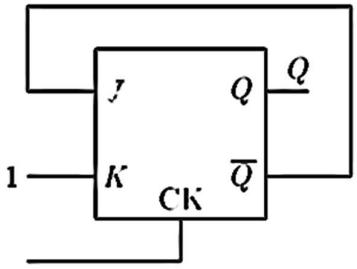
Q.4(a) X = 01110 and Y = 11001 are two 5-bit binary numbers represented in two's complement format. Find out the 6 bits sum of X and Y represented in two's complement format. [5]
Optimize the following Boolean functions F together with the don't-care conditions d in sum-of-products F (W, X, Y, Z) = Σm (5, 6, 11, 12).

Q.4(b) The logic function implemented by the circuit below is (ground implies a logic "0") [5]

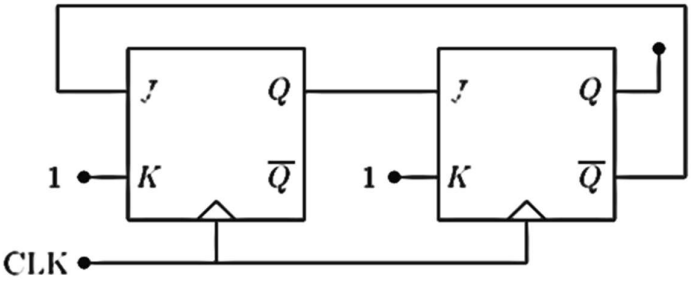


With the help of logic diagram and truth table, design a full Adder and realize a full Adder using only NAND gates

Q.5(a) In a J-K flip-flop we have J = Q and K = 1. Assuming the flip flop was initially cleared and then clocked for 6 pulses, what is the sequence at the Q output? [5]



Find out the maximum number of clock pulses the counter can count.



Q.5(b) Design a 3-bit serial in serial out shift register. [5]

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