BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO/2025

CLASS: M.TECH/PRE-PHD **SEMESTER: I**
BRANCH: ECE **SESSION: MO-2025**

SUBJECT: EC501 LOW POWER DEVICES & INTEGRATED CIRCUITS

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Express junction capacitance (Cd) and briefly explain each term used in it.	[5]	1	2
Q.1(b)	Sketch the plot of junction capacitance with respect to bias voltage for grading coefficient m = 0.5 and 0.33	[5]	1	3
Q.2(a)	Diagram the cross-sectional structure of an NMOSFET and PMOSFET taking a p-type lightly doped substrate. Sketch its I_{DS}-V_{DS} plot and I_{DS}-$V_{GS.}$	[2]	2	4
Q.2(b)	What are the various Regions of Operation of MOSFET. Mention the conditions of each region. Write down the drain-to-source current (I_{DS}) equation in each region.	[3]	2	3
Q.3(a)	What are the various Short Channel Effects? Explain Channel Length Modulation (CLM) and its effect on drain-to-source current a MOSFET.	[5]	3	1,4
Q.3(b)	Express the effect of the vertical field on the mobility and briefly explain each term in it.	[3]	3	2,4
Q.4(a)	Name various leakage currents in CMOS Devices. Express Dynamic Power Consumption and briefly explain each tern used in it.	[5]	4	1,3,5
Q.4(b)	Explain the mechanism of gate-induced drain leakage current (GIDL) and gate leakage current (I_G).	[5]	4	5
Q.5(a)	Schematize the layout of a 2-input NAND gate. Briefly explain how dynamic power consumption will be reduced, and circuit performance can be improved by your layout.	[2]	5	5,6
Q.5(b)	Briefly explain the various Leakage reduction Techniques in CMOS circuit design.	[3]	5	5

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