BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII/ADD**
BRANCH: ECE **SESSION : MO/2025**

SUBJECT: EC427 ASIC DESIGN

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Explain the orientation of VHDL. Define the ASIC.	[2]	1	2
Q.1(b)	Explain the important component of VHDL with suitable examples.	[3]	1	2
Q.2(a)	Define the entity with suitable examples.	[2]	1	2
Q.2(b)	Define the architecture with suitable example. Explain the classification of architecture with suitable examples.	[3]	1	3
Q.3(a)	Design the 1 bit full adder circuit at Gate level and write the VHDL & Verilog @HDL code for the same.	[2]	1	6
Q.3(b)	Design the Mux 4:1 circuit at Gate level and write the VHDL and Verilog HDL code for the same.	[3]	2	6
Q.4(a)	Define the process statement, signal assignment, and sequential statement.	[2]	2	5
Q.4(b)	Explain the loop and while statement with suitable examples. Differentiate between procedure and function with suitable examples.	[3]	2	2
Q.5(a)	Design the half adder circuit and write the test bench for the same.	[2]	2	6
Q.5(b)	Define the bus, generic, subprogram, package with suitable examples.	[3]	2	2

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