BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII/ADD**
BRANCH: ECE **SESSION : MO/2025**

SUBJECT: EC427 ASIC DESIGN

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Explain the Orientation of VHDL. Define the ASIC Design.	[5]	1	2
Q.1(b)	Describe the Basic Building Block and Important Component of VHDL.	[5]	1	2
Q.2(a)	Describe Entity and Architecture with Suitable examples. Also explain the types of Architecture.	[5]	2	2
Q.2(b)	Design 1 bit Full Adder Circuit and Write the VHDL & Verilog Code for the same.	[5]	2	6
Q.3(a)	Explain the Data types, file types, subprogram, function and procedures with suitable examples.	[5]	2	2
Q.3(b)	Design Mux 16:1 circuit and Write the VHDL and Verilog Code for the same.	[5]	3	6
Q.4(a)	Define the Subpackage, Package and Package Body and Case control flow statement with suitable examples.	[5]	2	2
Q.4(b)	Design 4 bit Up-down Counter using D Flip Flop and Write the VHDL & Verilog Code for the same.	[5]	3	6
Q.5(a)	Design Decoder 4:16 circuit using Decoder 2:4 and Write the VHDL & Verilog Code for the same.	[5]	4	6
Q.5(b)	Design the 4 bit Shift Register & Write the VHDL & Verilog Code for the same.	[5]	5	6

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