BIRLA INSTITUTE OF TECHNOLOGY, MESRA, PATNA CAMPUS
(MID SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : 7TH**
BRANCH: ECE **SESSION : MO/2025**

SUBJECT: EC425R1 LOW POWER VLSI CIRCUITS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Illustrate and explain the concept of channel length modulation.	[2]	1	3
Q.1(b)	A 1 GHz CMOS circuit drives a load capacitance of *20 fF* at V_{DD}=1.0 V. Calculate the dynamic power.	[3]	1	3
Q.2(a)	Explain junction leakage in nanometer MOSFETs with appropriate equations.	[2]	1	3
Q.2(b)	A processor operating at *VDD*=1.3*V* and with a capacitance C_L=3×10−12*F* has a delay of 120*ps*. The energy consumed per cycle is 10 pJ, and the power consumption is 5*mW*. If the supply voltage is reduced to 1.0*V*, the energy per cycle decreases by 40%, while the delay increases by 30%. Calculate the **Energy-Delay Product (EDP)** and **Power-Delay Product (PDP)** for both the original and scaled voltage conditions.	[3]	1	3
Q.3(a)	Discuss how body biasing techniques can reduce leakage currents.	[2]	1	3
Q.3(b)	Explain clock gating and its role in reducing dynamic power. Discuss power gating and its effect on leakage power.	[3]	1	3
Q.4(a)	Explain how transistor sizing affects power and delay in digital circuits.	[2]	2	3
Q.4(b)	A technology library offers a low-power NAND gate that consumes 30% less energy but increases delay by 20%. Discuss when to use it.	[3]	2	3
Q.5(a)	List advantages and challenges of multi-VDD designs.	[2]	2	3
Q.5(b)	Explain how algorithm-level optimizations can lead to energy-efficient hardware.	[3]	2	3

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