BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/2025**

SUBJECT: EC425 LOW POWER VLSI CIRCUITS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Distinguish between dynamic power, short-circuit power, and static power in CMOS circuits, with equations for each.	[5]	1	
Q.1(b)	A 45 nm NMOS shows linear-region current for small V_{DS}. Measured: I_D=40 μA_ with V_{GS}=0.8V, V_{DS}=50mV, W=1μm, L=45nm, C_{ox}=2.5 fF/μm², V_T=0.25V. (a)Compute μ_{eff}. (b) If velocity saturation reduces effective μ by 30% at high fields, estimate on-current penalty when VDS is large.	[5]	1	
Q.2(a)	Explain the concept of multiple supply voltages (multi-VDD) and discuss how it improves energy efficiency in SoC designs.	[5]	2	
Q.2(b)	A dual-VDD design has 40% of gates on critical paths (1.0 V) and 60% on non-critical paths (0.7 V). If total dynamic power at 1.0 V is 500 mW, compute new total power and percentage saving.	[5]	2	
Q.3(a)	Describe the role of Error Correction Codes (ECC) in reducing the minimum operating voltage of an SRAM array.	[5]	3	
Q.3(b)	Discuss the combined use of Raised-VSS and RBB in SRAM standby mode and explain how this improves leakage reduction without requiring triple-well technology.	[5]	3	
Q.4(a)	Explain why frequency scaling alone is not sufficient to reduce energy consumption, and justify the need for voltage scaling.	[5]	4	
Q.4(b)	Discuss voltage dithering (voltage hopping) in a continuous data-processing system. Explain how it helps in reducing average power consumption.	[5]	4	
Q.5(a)	Apply the CMOS inverter principle to design a low-voltage amplifier. Derive its small-signal gain and justify the choice of bias point for maximum gain with minimum power consumption.	[5]	5	3
Q.5(b)	Explain how an Operational Transconductance Amplifier acts as a direct-coupled differential voltage-controlled current source with the help of a neat circuit diagram.	[5]	5	3

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