

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**  
(MID SEMESTER EXAMINATION)

CLASS: B.TECH.  
BRANCH: ECE

SEMESTER: V/ADD  
SESSION: MO/25

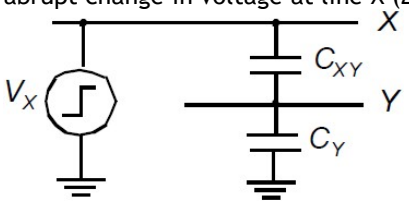
SUBJECT: EC319 VLSI SYSTEMS

TIME: 2:00 Hrs

FULL MARKS: 25

**INSTRUCTIONS:**

1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data handbook/Graph paper etc. to be supplied to the candidates in the examination hall.

- |   | Marks | CO | BL  |
|---|-------|----|-----|
| Q.1(a) For the static CMOS inverter fabricated in generic 0.25 $\mu\text{m}$ CMOS, the data sheet specifies the following parameters: $V_{IHmin} = 2.2\text{ V}$ , $V_{OHmin} = 2.5\text{ V}$ , $V_{ILmax} = 0.3\text{ V}$ , $V_{OLmax} = 0\text{ V}$ . Whereas the data sheet of pseudo-NMOS inverter fabricated in the same process specifies the following parameters: $V_{IHmin} = 2.2\text{ V}$ , $V_{OHmin} = 2.5\text{ V}$ , $V_{ILmax} = 0.3\text{ V}$ , $V_{OLmax} = 0.2\text{ V}$ . Calculate the HIGH noise margin ( $NM_H$ ) and the LOW noise margin ( $NM_L$ ) for both the static CMOS inverter and pseudo-NMOS inverter. Based on the estimation of noise margin, comment on both the logic families. | [2]   | 1  | 3   |
| Q.1(b) Sketch the voltage transfer characteristics (VTC) of a pseudo-NMOS inverter in generic 0.25 $\mu\text{m}$ process and mark important points on the curve.  | [3]   | 1  | 2   |
| Q.2(a) Briefly explain the effect of body bias on the threshold voltage ( $V_t$ ) of an NMOSFET. Explain using the equation of $V_t$ and the $V_t$ versus $V_{BS}$ plot.  | [2]   | 1  | 2,3 |
| Q.2(b) Write down various regions of operation of MOSFETs and their current equations.  | [3]   | 1  | 2,3 |
| Q.3(a) Explain the channel length modulation (CLM) effect with a suitable diagram. Write down nMOSFET's current equations to capture the CLM effect.  | [2]   | 1  | 4   |
| Q.3(b) Sketch the effect of $v_{DS}$ on $i_D$ in the saturation region in a short-channel nMOSFET. Mark the Early voltage on the sketch.  | [3]   | 2  | 3   |
| Q.4(a) What is an Interconnect? Define its pitch and aspect ratio. Substantiate your answer with a suitable diagram of the interconnect.  | [2]   | 2  | 2   |
| Q.4(b) What is crosstalk (clock feedthrough)?<br>Line X (maybe $M_1$ ) is coupled to wire Y by a parasitic capacitance $C_{XY}$ . Line Y (maybe substrate) has $C_Y$ as lumped parasitic capacitance to ground. Assume that the voltage at line X experiences a step change equal to $\Delta V_X$ . Express the impact of abrupt change in voltage at line X ( $\Delta V_X$ ) on victim line Y. Briefly explain.  | [3]   | 2  | 2,3 |
|    |       |    |     |
| Q.5(a) What are the various effects on the circuit behavior of the interconnect parasitics?   | [2]   | 2  | 2   |
| Q.5(b) Sketch the wire models for the circuit of Figure given below. While doing so consider most of the wire parasitics (except for inter-wire resistance and mutual inductance).  | [3]   | 2  | 3   |

