BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO-2025)

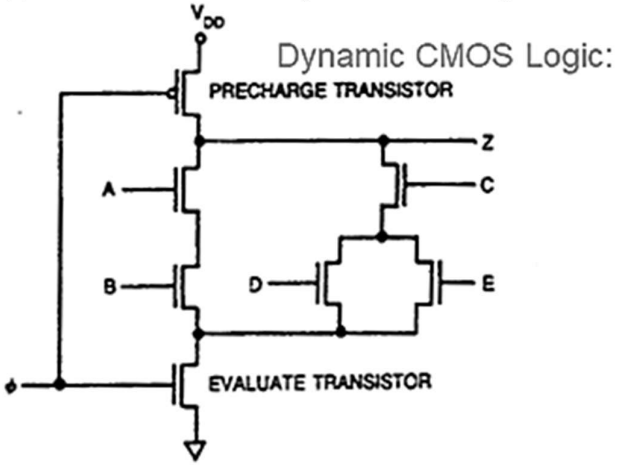
CLASS: B.TECH. **SEMESTER: V/ADD**
BRANCH: ECE **SESSION: MO/2025**

SUBJECT: EC319 VLSI SYSTEMS

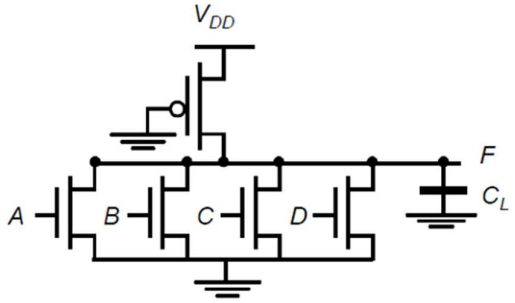
TIME: 3 HOURS **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and a total of 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates.**

				CO	BL
Q1	(a)	Briefly explain simple MOSFET capacitance models in the three regions of operation such as (a) Off region, (b) Linear region, and (c) Saturation region.	[5]	1	3
Q1	(b)	Write the expression of (a) dynamic power consumption, (b) Power-Delay Product (PDP) and (c) Energy-Delay Product (EDP). Explain each term in them.	[5]	1	2,3
Q2	(a)	Calculate the skin depth (δ) of aluminum wire ($\rho=2.7\times10^{-8}\,\Omega\cdot m$) routed through a surrounding dielectric with the permeability of free space (i.e., $\mu = 4\pi\times10^{-7}$ H/m) while carrying a current at 1 GHz.	[5]	2	4
Q2	(b)	Sketch a bidirectional pad with tristate buffer and input ESD protection circuit with minimum number of transistors. Briefly explain its operation.	[5]	2	3
Q3	(a)	Point out the various issues in Dynamic Design and explain charge sharing with a suitable diagram.	[5]	3	4
Q3	(b)	(i) Deduce the Boolean equations from the given transistor-level circuit diagram.	[5]	3	4



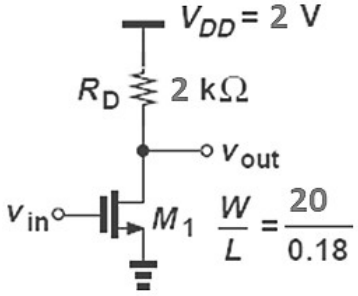
(ii) What function is realized by the circuit shown in Fig. below?



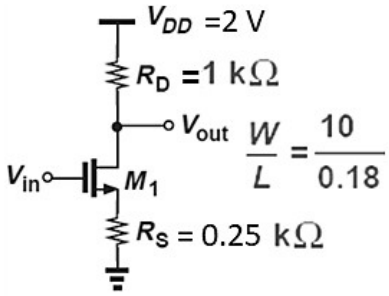
(iii) What are the disadvantages of the circuit in (ii).

PTO

Q4	(a)	Schematize transistor-level realization of a CMOS clocked SR flip-flop. Briefly explain its operation and sizing requirement.	[5]	4	4,6
Q4	(b)	Schematize transistor-level circuit of CMOS positive latch using transmission gates. Briefly explain its operation.	[5]	4	6
Q5	(a)	Evaluate the small-signal voltage gain of the CS stage shown in Fig. if I_D = 0.5 mA, $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5 V, and λ = 0. Verify that M_1 operates in saturation.	[5]	5	5,6



Q5	(b)	Estimate the small-signal parameter g_m and voltage gain of the CS stage with load resistor R_D and source degeneration resistor R_S as shown below if I_D = 1 mA, $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5 V, and λ = 0. Verify that M_1 operates in saturation.	[5]	5	6



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