BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

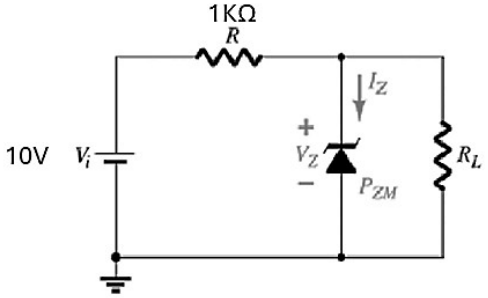
CLASS: BTECH **SEMESTER : I**
BRANCH: ECE/EEE/CSE/AIML **SESSION : MO/2025**

SUBJECT: EC24101 BASIC ELECTRONICS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Using your understanding of semiconductor behavior, explain how VI characteristics of a silicon diode change when the temperature increases from 25°C-75°C.	[2]	1	3
Q.1(b)	Explain the construction and working of a PN junction diode and describe how depletion region is formed with neatly labeled energy band diagram.	[3]	1	2
Q.2(a)	A germanium diode carries a current of 1mA at room temperature when a forward bias of 0.15V is applied. Estimate the reverse saturation current at room temperature. (For Germanium, η=1)	[2]	1	3
Q.2(b)	Explain the construction and working of center tap full wave rectifier with circuit diagram. Derive the rectification efficiency for it.	[3]	1	2,3
Q.3(a)	Both Zener and Avalanche breakdown mechanisms are used in voltage regulation circuits. Evaluate the suitability of each mechanism for low-voltage and high-voltage applications.	[2]	1	5
Q.3(b)	In the circuit shown below, V=10V, R=1KΩ, and breakdown voltage of Zener diode is 6V. Determine I_z if (i)R_l=100Ω and (ii) R_l=9KΩ	[3]	1	4



Q.4(a)	Derive the relationship between the current gain coefficients α (common-base), ß (common-emitter), and γ (common-collector) of a BJT.	[2]	2	3
Q.4(b)	Draw the circuit diagrams of an NPN transistor in Common-Base (CB), Common-Collector (CC), and Common-Emitter (CE) configurations. Label all terminals, input and output.	[3]	2	2
Q.5(a)	Draw and explain the fixed-bias circuit for an NPN transistor in common-emitter configuration. Using circuit analysis, derive the expressions for the zero-signal collector current and collector-to-emitter voltage (V_{CE}).	[2]	2	2,3
Q.5(b)	Design a fixed bias circuit for a CE transistor amplifier such that the operating point is V_{CE}=8V and I_c=2mA. The circuit is supplied with a fixed 15V DC supply and silicon transistor with ß=100.	[3]	2	6

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