

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)**

CLASS: B.TECH
BRANCH: CSE/AIML

SEMESTER : III/ADD-
SESSION : MO/2025

SUBJECT: CS24205 / CS235 COMPUTER ORGANIZATION AND ARCHITECTURE

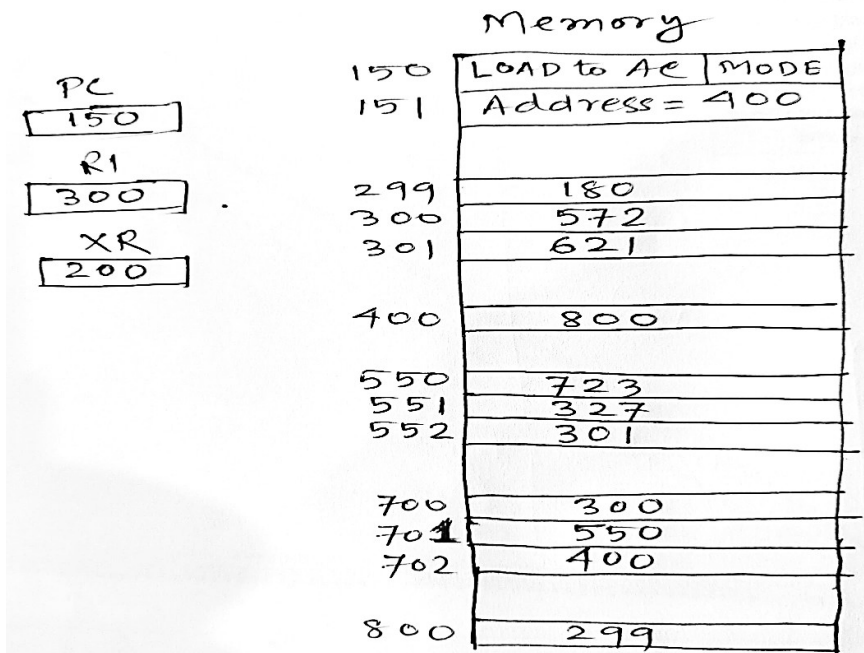
TIME: 02 Hours

FULL MARKS: 25

INSTRUCTIONS:

1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates

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|--|-----|----|----|
| Q.1(a) Why implicit normalization is better than explicit normalization in context of floating-point representation. Use binary equivalent of 5.625. | [2] | 1 | 3 |
| Q.1(b) Using Booths multiplication algorithm multiply (9)x(-13) | [3] | 1 | 3 |
| Q.2(a) Two computers use same instruction set architecture. Computer X has a clock cycle time of 300 ps and a CPI of 2.5 for some program and computer Y has a clock cycle time of 400 ps and a CPI of 1.5 for the same program. Which computer is faster for this program and by how much? | [2] | 1 | 3 |
| Q.2(b) Design a circuit that can take 3 bit binary number as input and generate an output which is the square of the input number. Show the Truth table, K-map (for the required bits) and the circuit. | [3] | 1 | 3 |
| Q.3(a) Explain the details of Von Neumann architecture . | [2] | 1 | 1 |
| Q.3(b) The two-word instruction at address 150 and 151 is a "load to AC" instruction with an address field equal to 400. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. PC has the value 150 for fetching this instruction. The content of processor register R1 is 300, and the content of an index register XR is 200. AC receives the operand after the instruction is executed. Show the effective address and content of AC for Memory indirect, Immediate and Relative addressing modes. | [3] | 2 | 3 |



- Q.4(a) With a suitable example, show how the subroutines are executed step by step in the context of registers usage. [2] 2 3
- Q.4(b) Explain the data path in a processor with the help of a neat diagram. [3] 2 1
- Q.5(a) A memory unit has a capacity defined as:
Capacity/size = (Number of Words)×(Number of Bits per Word)
Calculate the number of address lines and data lines required for a memory of size 64K×16. [2] 2 3
- Q.5(b) Justify the statement: “Control lines are individually unidirectional but collectively bidirectional” with a suitable diagram. [3] 2 1

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