BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : III/ADD**
BRANCH: CSE/IT **SESSION : MO/2025**

SUBJECT: CS24205 COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Design a 4-bit carry look ahead adder circuit with operational details.	[5]	1	3
Q.1(b)	Consider the three floating point numbers A, B, and C stored in registers R_A, R_B, and R_C respectively as per IEEE-754 single-precision floating point format. The 32-bit content stored in these registers (in hexadecimal form) are as follows. Verify the following (i) C = A + B and (ii) (B-C)>0	[5]	1	2

R_A	R_B	R_C
0XC1400000	0X42100000	0X41400000

Q.2(a) Given a sequence of code with their addresses and content of some memory locations. Assume each instruction takes 2 bytes memory: [5] 2 3

CODE

```
MAIN (starts at 1000)
1000  LOAD  A, 5000
1002  CALL  SUB1
1004  ADD   A, 2
1006  STORE A, 6000
1008  HALT

SUB1 (starts at 1400)
1400  ADD   A, 1
1402  CALL  SUB2
1404  ADD   A, 10
1406  RETURN

SUB2 (starts at 1800)
1800  ADD   A, 7000    ; add value stored at memory location 7000
1802  RETURN
```

Memory Location with initial content

```
mem[5000] = 6
mem[7000] = 9
mem[6000] = 5
```

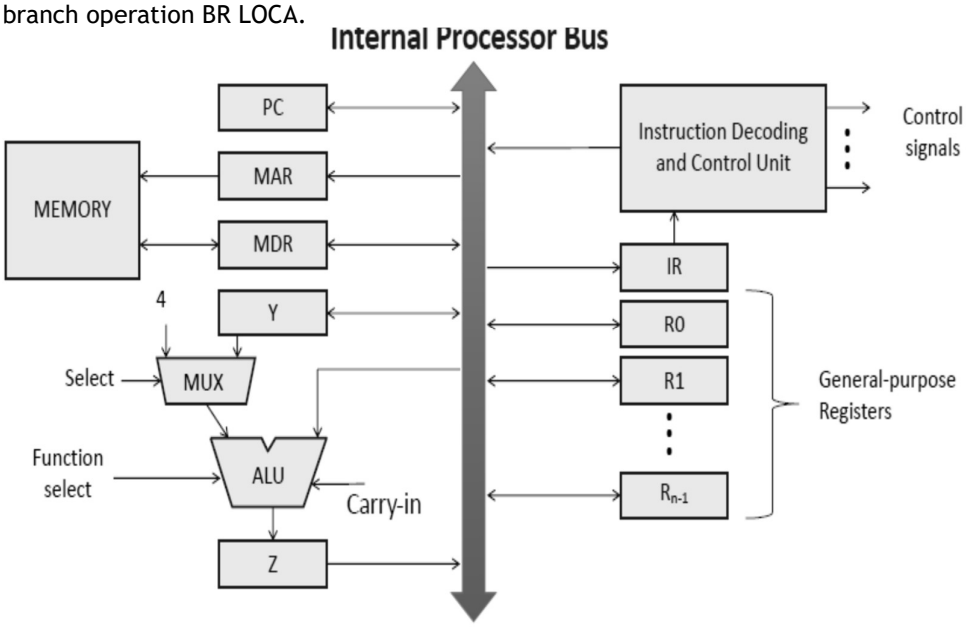
Find:

1. The sequence of instruction addresses executed. (2 marks)
2. The final content of accumulator A and mem[6000]. (2 marks)
3. At the start of this program PC (Program Counter) contains 1000. What will be content of PC when it is executing last but one statement of the code. (1 marks)

Q.2(b) With proper example explain the Little and Big Endian representation of data. How they are different in data accessing for read or write operation? Explain properly [5] 2 2

PTO

Q.3(a) Consider the following single bus architecture and generate the micro-operations for branch operation BR LOCA. [5] 3 4



Q.3(b) Consider a five-stage pipeline having phase duration 50ns, 80ns, 70ns, 40ns and 90ns. Given buffer delay is 10ns. Calculate (i) Pipeline cycle time, (ii) non-pipeline execution time, (iii) Speed up ratio, (iv) Pipeline time for 100 tasks and (v) Sequential time for 100 tasks. [5] 3 3

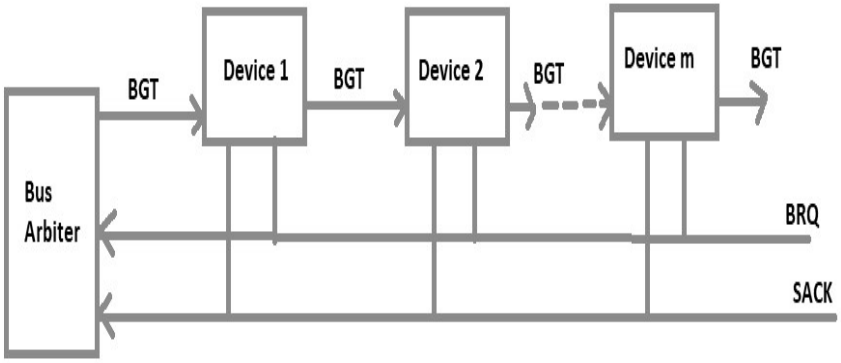
Q.4(a) Design the schemes to increase [5] 4 3
(i)the word size of a RAM by a factor of 4 and
(ii)Increase the number of words stored in a RAM by a factor of 4

Q.4(b) A 4-way set associative cache memory has a total capacity of 32 KB. The block size is 8 words, and each word consists of 32 bits. The physical address space of the system is 6 GB. Determine the number of bits required for each of the following fields in the physical address used for cache mapping: [5] 4 3

1. Tag field
2. Block (Set) no field
3. Block offset (word/byte offset) field

Q.5(a) Explain the working principle of DMA (step by step) with suitable figure. [5] 5 3

Q.5(b) (i) Which type of Bus arbitration method is shown in the following figure? What are the demerits of this method? [5] 5 3



(ii) Differentiate between Multiprocessor and Multicomputer with respect to structural and behavioral nature.

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