BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

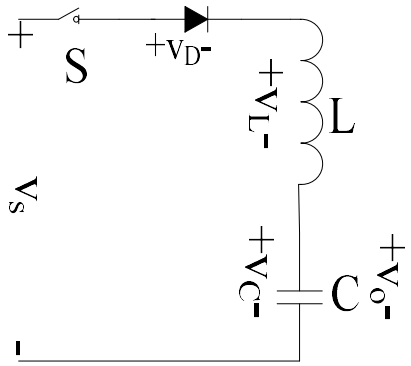
CLASS: M.Tech **SEMESTER : I**
BRANCH: Electrical Engineering **SESSION : MO/2024**

SUBJECT: EE507 ADVANCED POWER ELECTRONICS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Draw cross-sectional diagram of POWER MOSFET. Draw switching characteristics of Power MOSFET.	[5]	1	2
Q.1(b)	In the diode and LC network, the capacitor is charged to voltage Vo with upper plate positive. Switch S is closed at t=0. Derive expressions for current through and voltage across C. Assume other data.	[5]	1	2



Q.2(a)	With the help of equivalent circuit diagram illustrate operating principle of Half bridge converter along with the theoretical waveforms with relevant equations	[5]	2	3
Q.2(b)	Illustrate the operation of the forward converter with demagnetizing winding of 100W. Assume other specifications.	[5]	2	3
Q.3(a)	Examine the operating principle of cascaded multilevel converter with a neat circuit diagram and relate with other multilevel inverters	[5]	3	4
Q.3(b)	Analyse multiple pulse width modulation technique and compare with sinusoidal PWM technique	[5]	3	4
Q.4(a)	Evaluate the Zero Voltage Switching Resonant Converter with the theoretical waveforms of Capacitor voltage and inductor current, derive the resonant capacitor voltage during resonant state.	[5]	4	5
Q.4(b)	Derive the relation of current through resonant inductor during mode 2 and mode 3 i.e., during resonant state.	[5]	4	5
Q.5(a)	Design a IGBT gate drive circuit	[5]	5	6
Q.5(b)	Devise an intelligent power module control strategy for an inverter	[5]	5	6

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