BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2024)

CLASS: BTECH **SEMESTER : 5th**
BRANCH: EEE **SESSION : MO/2024**

SUBJECT: EE353 POWER ELECTRONICS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Name an uncontrollable semiconductor switch and a controllable semiconductor switch. Draw their proper symbols.	[2]	1	1
Q.1(b)	Define Safe Operating Area of a semiconductor switch. Give any one example.	[3]	1	1
Q.2(a)	Explain turning on mechanism of a thyristors using two transistor topology.	[2]	2	2
Q.2(b)	Compare a Power MOSFET with an IGBT and illustrate the major differences.	[3]	2	2
Q.3(a)	Apply class B commutation on a thyristor and explain its turning-off mechanism by drawing the waveform of commutating current and capacitor voltage.	[2]	3	3
Q.3(b)	Identify the most economical category of commutation of thyristor. Justify your response.	[3]	3	3
Q.4(a)	Analyze the dynamic characteristics of a power diode and explain the impact of di/dt on the reverse recovery time.	[2]	4	4
Q.4(b)	Illustrate the major challenge in the series operation of multiple thyristors for establishing dynamic balancing of voltage across the individual thyristor in the string. Provide a feasible solution with proper reasoning.	[3]	4	4
Q.5(a)	Design an AC to DC power converter with controllable output voltage feeding a resistive load.	[2]	5	5,6
Q.5(b)	Evaluate the ideal efficiency of an AC to DC power converter feeding a resistive load, by drawing the AC supply voltage waveform, Supply Current waveform, Load voltage waveform, Load current waveform, and Voltage waveform across the semiconductor switch. Assume ideal switching operation with no switching loss or conduction loss.	[3]	5	5,6

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