BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: MTECH **SEMESTER : I**
BRANCH: ECE **SESSION : MO/2024**

SUBJECT: EC501 LOW POWER DEVICES & INTEGRATED CIRCUITS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Generate the Conductor, Insulator and Semiconductor with energy band diagram. Draw the diagram of PN junction and establish the relation of space charge region. Explain the Oxidation, photolithography, ion-implantation and metallization.	[5]	1	7
Q.1(b)	Explain the capacitance in an abrupt PN junction, depletion layer capacitance with arbitrary doping profile. Define doping and etching.	[5]	1	2
Q.2(a)	Explain the drain current equation of NMOS transistor. Show the ID-VD Characteristics of NMOS transistor and show the working region of Transistor.	[5]	2	2
Q.2(b)	Describe the Fabrication process of CMOS Inverter Circuit, Show the comparative layout of CMOS Inverter circuit fabricated structure. Derive the aspect ratio of CMOS Inverter circuit.	[5]	2	2
Q.3(a)	Describe the channel length modulation effect, hot carrier injection and mobility degradation.	[5]	2	2
Q.3(b)	Design the circuit Y= (ABC+DEF+GHI)' using CMOS and Pseudo NMOS Technology.	[5]	2	6
Q.4(a)	Describe Subthreshold leakage current, Gate Leakage current, gate induced drain leakage current.	[5]	3	2
Q.4(b)	Design the X-OR Gate using TG (Transmission Gate) logic. Explain the SOI technique with flow of important process.	[5]	3	6
Q.5(a)	Explain the Design rules. Design the layout of 2-input NAND Gate and 2- input NOR Gate with spacing rules.	[5]	4	2
Q.5(b)	Write the VHDL Code of 1-bit Half Adder. Design the CMOS Operational Amplifier circuit and explain the importance of current mirrors.	[5]	4	5

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