CLASS: B.Tech   SEMESTER: VII
BRANCH: ECE   SESSION: MO/2024

SUBJECT: EC427 ASIC DESIGN

TIME: 2 HOURS   FULL MARKS: 25

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates.

			CO	BL
Q.1(a)	Explain the basic terminologies of VHDL.	[2]	CO1, CO2	L1
Q1(b)	Write the VHDL code for a Full Subtractor.	[3]	CO1, CO2	L2
Q2(a)	Write a note on test benches.	[2]	CO1, CO2	L1
Q2(b)	Explain the process statement with the help of example. Differentiate between signal and variable assignment.	[3]	CO1, CO2	L3
Q3(a)	Differentiate between sequential statements and the concurrent statements?	[2]	CO1, CO2	L3
Q3(b)	Differentiate between the following: 1) signal and variable 2) sensitivity list and WAIT statement	[3]	CO1, CO2	L1
Q4(a)	Write the VHDL code for the given state diagram, using behavioral modeling:	[2]	CO1, CO2	L4

			CO	BL
Q4(b)	Explain in detail the concept of structural modeling in VHDL with an example of full adder.	[3]	CO1, CO2	L3
Q5(a)	Differentiate between array types and record types.	[2]	CO1, CO2	L1
Q5(b)	Write VHDL code for Gray to Binary and Binary to Gray encoders.	[3]	CO1, CO2	L3