BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2024)

CLASS: BTECH **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/2024**

SUBJECT: EC425 R1 LOW POWER VLSI CIRCUITS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Define leakage current in a nanometer MOSFET.	[2]	1	2
Q.1(b)	Apply the alpha power model to calculate the current in a MOSFET operating in velocity saturation.	[3]	1	3
Q.2(a)	Explain the impact of process variation on the threshold voltage of MOSFETs.	[2]	1	2
Q.2(b)	How would you optimize a circuit design to reduce the energy-delay product for a given application?	[3]	1	3
Q.3(a)	Describe the benefits of using multiple supply voltages in a low-power design.	[2]	2	2
Q.3(b)	Apply dynamic power optimization techniques to a clock distribution network in a digital circuit to reduce power consumption.	[3]	2	3
Q.4(a)	Discuss how transistor stacking can reduce leakage currents in CMOS circuits.	[2]	2	2
Q.4(b)	Analyze how alternative topologies could reduce power consumption in a specific architecture.	[3]	2	3
Q.5(a)	Explain the difference between L1, L2, and L3 caches in modern processors.	[2]	3	2
Q.5(b)	Apply transistor sizing to a 6T SRAM cell to optimize for both stability and power consumption.	[3]	3	3

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