BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VIITH**
BRANCH: ECE **SESSION : MO/2024**

SUBJECT: EC425 LOW POWER VLSI CIRCUITS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Discuss the different types of leakage currents in nanometer MOSFETs. How do these leakage currents contribute to static power dissipation in ultra-low-power applications?	[5]	1	3
Q.1(b)	Using Alfa power model, calculate the drain current of a short channel p-MOS if V_T = 0.3 V, V_{GS} = -3.7V, W/L=4, μ = 350cm^2 / Vs, ε = 3.9 *8.854 *10 $^{-12}$ F/N, t_{ox} = 100 Å and α = 1.3.	[5]	1	3
Q.2(a)	Analyze the concept of transistor stacking in CMOS circuits. Explain how stacking transistors in series can help reduce subthreshold leakage currents and improve static power efficiency.	[5]	2	3
Q.2(b)	A CMOS circuit operates with V_{DD}=1.2V, a load capacitance of C_L=6×10^{-12}F, a delay of 100*ps*, and consumes 5 pJ energy per cycle with an average power consumption of 2*mW*. If the supply voltage is reduced to 1.0*V*, causing a 20% increase in delay and a 30% decrease in energy per cycle, calculate the Energy-Delay Product (EDP) and Power-Delay Product (PDP) for both the initial and scaled voltage conditions. Compare the two products and analyze the impact of voltage scaling on both energy efficiency and power-delay trade-off.	[5]	2	3
Q.3(a)	Analyze the challenges in interconnect design for modern ICs as technology scales down to the nanometer regime.	[5]	3	3
Q.3(b)	Explain the wire energy-delay trade-off in interconnects. what design techniques can be used to optimize the wire energy-delay trade-off in high-performance ICs?	[5]	3	3
Q.4(a)	Discuss the concept of Reverse Body Bias (RBB) and its effect on reducing power consumption in standby mode.	[5]	4	3
Q.4(b)	Explain how clock gating can be used to reduce dynamic power consumption in circuits during standby mode. Discuss the advantages of clock gating over other methods of power reduction.	[5]	4	3
Q.5(a)	For a CMOS inverter-amplifier operating at V_{DD}=1.0*V* with transistor parameters W/L=10 μm/0.5 μm, threshold voltage Vth=0.3 V, ß=150 μA/V^2, and load resistance R_L=10 kΩ, calculate the maximum transconductance-to-current ratio (g_m/I_D) for the transistor when the drain current is I_D=100*μA*, the voltage gain *Av* of the inverter-amplifier, and the input and output voltage swing assuming the transistor operates in saturation.	[5]	5	3
Q.5(b)	Analyze the voltage transfer characteristics of a CMOS inverter amplifier in the weak inversion region. What are the trade-offs involved in using this amplifier in low-voltage applications?	[5]	5	3

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