BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

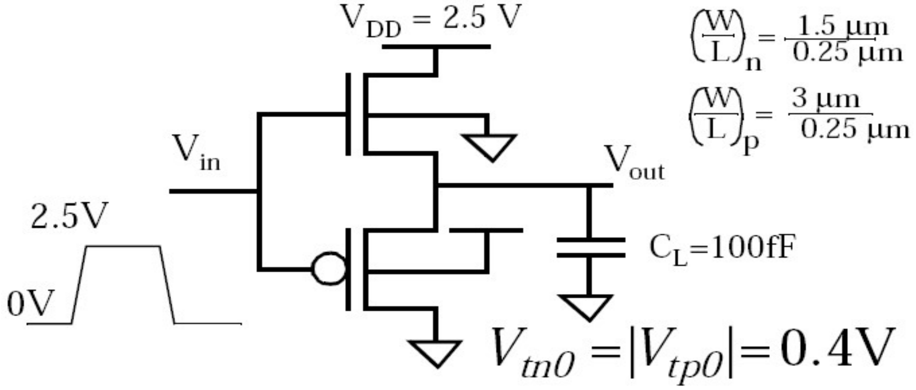
CLASS:	**BTECH**	**SEMESTER: V**
BRANCH:	**ECE**	**SESSION: MO/24**

SUBJECT: EC319 VLSI SYSTEMS

TIME:	**2:00 Hrs**	**FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data handbook/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	The data sheet of a CMOS inverter specifies the following parameters: V_{IHmin} =700 mV, V_{OHmin} = 900 mV, V_{ILmax} = 300 mV, V_{OLmax} = 100 mV. Calculate the HIGH-state noise margin (NM_H) and the LOW-state noise margin (NM_L).	[2]	1	3
Q.1(b)	Describe the switching threshold (V_M) of a CMOS inverter. Explain how its value is obtained graphically. What is the desired value of V_M for a CMOS inverter in 0.25 µm process?	[3]	1	2
Q.2(a)	Write down the (V_{OL}) and (V_{OH}) of the low swing driver shown in the Figure below. Explain why the output voltage swing (V_{out}) is not rail-to-rail. Assume λ=0.	[2]	1	2,3



Q.2(b)	Write down various regions of operation of MOSFETs and their current equations. Explain the channel length modulation (CLM) effect with a suitable diagram.	[3]	1	2,3
Q.3(a)	Deduce the expression of energy E_{VDD}, taken from V_{DD} during the 0→1 transition of the output node.	[2]	1	4
Q.3(b)	Briefly explain the power-delay product (*PDP*). Calculate the power-delay product (*PDP*) of a CMOS inverter designed in a generic 0.25-µm CMOS process having a load capacitance C_L of 6 *fF*.	[3]	2	3
Q.4(a)	What is an Interconnect? Define its pitch and aspect ratio. Substantiate your answer with a suitable diagram of the interconnect.	[2]	2	1
Q.4(b)	Define crosstalk (clock feedthrough)? Consider that a clock wire and a victim wire are routed side-by-side. What impact is found on the victim wire if the clock in the clock wire makes a high-to-low transition? Substantiate your answer with a suitable diagram and explain it.	[3]	2	1
Q.5(a)	What is skin effect and skin depth? Formulate skin depth mentioning each term in minimum words.	[2]	2	6
Q.5(b)	Calculate the skin depth (δ) of aluminum wire ($\rho=2.7\times10^{-8}\ \Omega\cdot m$) routed through a surrounding dielectric with the permeability of free space (i.e., $\mu = 4\pi\times10^{-7}$ H/m) while carrying a current at 1 GHz.	[3]	2	4

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