

BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO-2024)

CLASS: BTECH.
BRANCH: ECE

SEMESTER: V
SESSION: MO/2024

SUBJECT: EC319 VLSI SYSTEMS

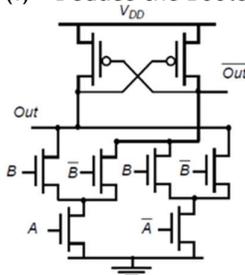
TIME: 3 HOURS

FULL MARKS: 50

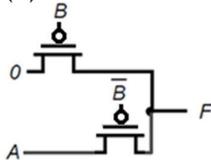
INSTRUCTIONS:

1. The question paper contains 5 questions each of 10 marks and a total of 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates.

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|---|-----|----|------|
| Q1 (a) Write the main reason for the occurrence of (i) velocity saturation, (ii) hot carrier injection, and (iii) mobility degradation. (iv) Explain the velocity saturation effect. Substantiate your answer with a suitable diagram. | [5] | 1 | 2,3 |
| Q1 (b) Compute the total value of load capacitance (C_L) of a loaded inverter and explain it with a suitable diagram. | [5] | 1 | 2,3 |
| Q2 (a) (i) A wire, which is 10 cm long and 1 μm wide, is routed on the polycide, the sheet resistance of which is 4 Ohm-per-square. Compute the total resistance of the wire. (ii) Write down the desired characteristics of the input pad. (iii) Schematize input pad electrostatic discharge (ESD) protection circuit. | [5] | 2 | 3, 6 |
| Q2 (b) Sketch gate-level schematics of a tristate buffer, which may be used in an output pad, and explain its operation. | [5] | 2 | 3 |
| Q3 (a) Sketch the transistor-level circuit diagram of (i) a 3-input pseudo-NMOS NAND gate and (ii) a 4-input pseudo-NMOS NOR gate. (iii) What disadvantage is encountered for all high input signals in the pseudo-NMOS NAND gate? | [5] | 3 | 3 |
| Q3 (b) (i) Deduce the Boolean equations from the given transistor-level circuit diagram. | [5] | 3 | 4 |



(ii) What function is realized by the circuit shown in Fig. below?



(iii) What is the numerical value of F when input signals $A = B = 0\text{ V}$ are applied after the application $A = B = 1\text{ V}$? Assume that $V_{tp} = -0.4\text{ V}$.

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|--|-----|---|-----|
| Q4 (a) (i) Schematize dynamic positive edge-triggered (master/slave) register. | [5] | 4 | 5,6 |
| (ii) Argue in favour of the dynamic positive edge-triggered (master/slave) register for its advantages and applications. | | | |
| (iii) Criticize the dynamic positive edge-triggered (master/slave) register for its disadvantages. | | | |

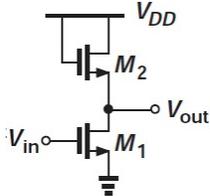
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Q4 (b) Explain the approach of optimizing sequential circuits with an example of datapath for the computation of $\log(|a+b|)$. Substantiate your answer with a suitable diagram and pipelined computation table for a brief explanation.

[5] 4 4

Q5 (a) A MOSFET-based circuit is given below:

[5] 5 2,3,5,6



(i) In the given circuit, identify the diode-connected MOSFET. (ii) Determine the region of operation of the diode-connected MOSFET. (iii) Estimate the resistance offered by this diode-connected MOSFET, if $\lambda \neq 0$. (iv) Express the output impedance of the given circuit if $\lambda \neq 0$. (v) Evaluate the voltage gain of the given circuit if $\lambda \neq 0$.

Q5 (b) Schematize the CS stage with load resistor R_D and source degeneration resistor R_S . Ignoring the channel-length modulation effect, schematize its small-signal model and derive the expression of its voltage gain if $\lambda = 0$.

[5] 5 6

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