BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER: V/ADD**
BRANCH: ECE **SESSION: MO/2024**

SUBJECT: EC303 MICROPROCESSORS AND MICROCONTROLLERS

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions, each of 10 marks and a total of 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Explain the following i) Fetch Execute Overlap (FEO) and its advantage with the help of an example ii) Addressing modes of 8085 with suitable examples of each mode	[5]	1	2
Q.1(b)	There is no 16-bit ALU available in 8085 µp, so how is a double-byte addition done using an HL register pair? Explain. Two words of 16 bits reside at locations 2400 H (WORD1) and 2420 H (WORD2), respectively. If the number of 1's in the first word is more than that of the second one, place a 00H at location 2450H; otherwise, FFH and put EEH if they are equal.	[5]	2	3
Q.2(a)	Differentiate the following with their relative merits and demerits. i) Memory-mapped I/O and I/O mapped I/O ii) Interrupt-driven I/O and Programmed (status-check) I/O.	[5]	2	3
Q.2(b)	Write down all the steps taken by the 8085 µp if an interrupt is received at the INTR pin. Write an 8085-based ALP to input 20 bytes using RST 6.5 through port no. 40H. Write an interrupt service routine to input each byte, convert it to BCD and store it in a location starting from 2500H. Ensure the interrupt is disabled after receiving 20 bytes.	[5]	2	3
Q.3(a)	What do you understand by even and odd memory addressing in 8086 µp? Why is the combination of $\overline{BHE}$ (Active low) and A_0 necessary for accessing even and odd address banks of memory, and what role does it play in minimising bus cycles during memory operations?	[5]	4	2
Q.3(b)	Differentiate the following i) Minimum & Maximum mode of operation of 8086. ii) Control & status flags of the flag register of 8086.	[5]	4	1
Q.4(a)	Write down the different modes of operation of 8255 PPI. The room temperature measured by a temperature sensor is reflected on the D_0 and D_1 inputs connected to PA_0 and PA_1 pins of 8255 PPI. The room temperature is controlled by a cooler, fan, and heater, and an appropriate action to be taken based on the room temperature is mentioned against each reading below.	[5]	3	4

Temperature	Sensor output		Action to be taken		
	D_1	D_0	Cooler	Heater	Fan
< 15^0C	0	0	OFF	ON	OFF
15 -20^0C	0	1	OFF	OFF	OFF
20 -30^0C	1	0	OFF	OFF	ON
> 30^0C	1	1	ON	OFF	OFF

PA2, PA3, and PA4 pins of the same 8255 PPI control the cooler, heater, and fan. Write an 8085-based ALP to implement the same.

Q.4(b)	Write a program to generate a train of square waves having a frequency of 100 Hz using an 8253 timer. Assume CLK1 frequency is 5 MHz, and PC_5 of 8255 is connected to GATE1 of 8253 timer.	[5]	3	4

PTO

Q.5(a)	Explain the following in the context of 8051 µc i) stack operation with the help of an example ii) operation of the pins used while an external memory is interfaced	[5]	4	2
Q.5(b)	Differentiate between General Purpose RAM (GPR) and Special Function RAM (SFR). Explain the memory organisation for the 128-byte internal RAM of 8051 µc.	[5]	4	3

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