BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2024)

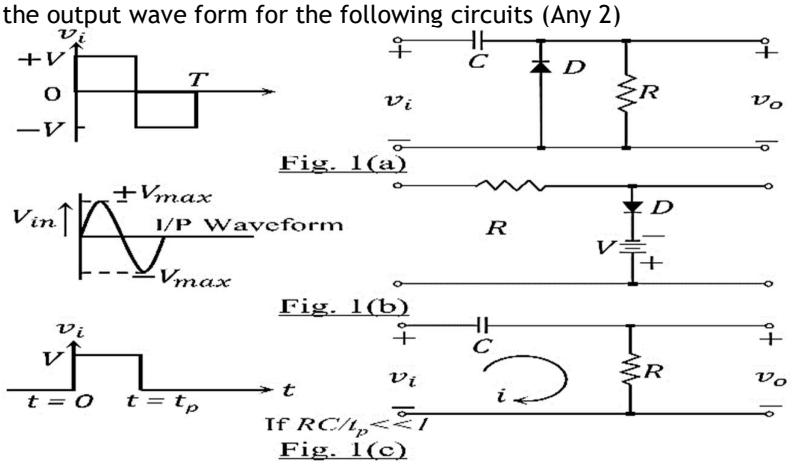
CLASS: BTECH **SEMESTER : III/ADD**
BRANCH: ECE **SESSION : MO/2024**

SUBJECT: EC211ANALOG CIRCUITS

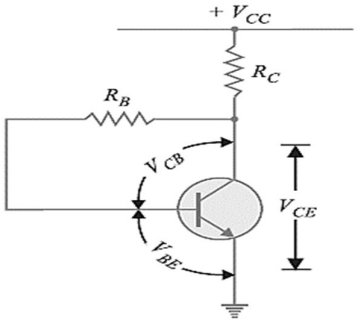
TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Draw the output wave form for the following circuits (Any 2)	[2]	1	2



Q.1(b)	It is required to set the operating point by biasing with the circuit given at I_C = 1mA, V_{CE} = 8V. i)If ß = 100, V_{CC} = 12V, V_{BE} = 0.3V, how will you do it ? (ii) What will be the new operating point if ß = 50, all other circuit values remaining the same ?	[3]	2,3	3



Q.2(a)	Which transistor configuration (CE, CB or CC) provides: i. Lowest voltage gain ii. Highest input impedance iii. Lowest input impedance iv. Lowest output impedance	[2]	1	2
Q.2(b)	Draw small signal diagram of CE amplifier (without emitter resistor) and derive its voltage gain and input impedance.	[3]	3	4
Q.3(a)	Draw the frequency response of a Transistor amplifier. What are the role of capacitors in different frequency band.	[2]	3	3
Q.3(b)	Derive the voltage gain of CE amplifier in low frequency domain considering the effect of only coupling capacitor (C1) connected at the base terminal.	[3]	1,2,4	4

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Q.4(a)	A three-stage amplifier has a first stage voltage gain of 100, second stage voltage gain of 200 and third stage voltage gain of 20dB. Find the overall voltage gain in decibels.	[2]	1,2,3	3
Q.4(b)	Briefly Explain the working principle of Darlington pair circuit? What are its advantages?	[3]	1,2,3	3
Q.5(a)	Illustrate the origin of the internal capacitances Cπ and Cμ. State Miller theorem.	[2]	3,4	3
Q.5(b)	Draw the low frequency model of RC -coupled amplifier. Derive the expression for f_L .	[3]	1,2,4	4

OR

A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is Vce = 10V and Ic = 1mA : hie = 1k Ω; hoe =25μA/V; hre = $2x10^{-4}$; hfe = 50. Determine (i) input impedance (ii) current gain and (iii) voltage gain iv) output impedance using exact and approximate analysis. The load seen by the transistor is R_L = 1000 Ω and Voltage source of internal resistance Rs=800Ω.

:::::24/09/2024 E:::::