

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2024)**

**CLASS: B. TECH.
BRANCH: ECE/CSE/AI ML/EEE**

**SEMESTER : III
SESSION : MO/2024**

SUBJECT: EC203 DIGITAL SYSTEM DESIGN

TIME: 02 Hours

FULL MARKS: 25

INSTRUCTIONS:

1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates

		CO	BL
Q.1(a) Let R_1 , R_2 , and R_3 are 4-bit registers that store signed numbers in 2's complement form. Say, $R_1=1100$ and $R_2=1011$, and the result of (R_1+R_2) is stored in R_3 . Does R_3 contain a valid data? Justify your answer.	[2]	1,2	1
Q.1(b) (i) Convert the decimal number 0.456 into its octal equivalent. (ii) In a number system of base r , the equation $x^2-12x+37=0$, has $x=8$ as one of its solutions. Calculate the value of r .	[1+2]	1,2	2
Q.2(a) Explain the following parameters regarding logic gates: (i) Noise Margin (ii) Fan out.	[2]	1,2	1
Q.2(b) Explain the working of a standard TTL-inverter circuit with diagram.	[3]	1,2	2
Q.3(a) What are the advantages of CMOS logic family? Implement the logic function, $Y=AB+C$ using CMOS logic (Complemented inputs allowed).	[2]	1,2	1
Q.3(b) Minimize the following Boolean function using K-Map and further implement using NAND gates (upto three inputs) only. $Y(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 8) + d(10, 11, 12, 13, 14, 15)$	[3]	1,2	2
Q.4(a) Convert the following Boolean function into maxterm representation: $Y(A, B, C)=(A+B)(B+C)(A+C')$	[2]	1,2	1
Q.4(b) Minimize the following Boolean function using K-Map and further implement using NOR gates (upto three inputs) only. $F(A, B, C, D) = \pi(1, 2, 3, 5, 8, 9, 10, 11). d(7, 15)$	[3]	1,2	2
Q.5(a) Define entity and architecture in VHDL coding with an example.	[2]	1,2	1
Q.5(b) A digital system has a 3-bit input from 000 to 111. Design a logic circuit that produces a high output whenever the equivalent decimal input is an odd number. Perform the steps using K-Map simplification and realization with NAND gates.	[3]	1,2	2

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