

**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)**

**CLASS: BTECH.
BRANCH: ECE+CS+AIML+EEE**

**SEMESTER : III/ADD
SESSION : MO/2024**

SUBJECT: EC203 DIGITAL SYSTEM DESIGN

TIME: 3 Hours

FULL MARKS: 50

INSTRUCTIONS:

1. The question paper contains 5 questions each of 10 marks and total 50 marks.
 2. Attempt all questions.
 3. The missing data, if any, may be assumed suitably.
 4. Before attempting the question paper, be sure that you have got the correct question paper.
 5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.
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|--------|---|------------|----|
| Q.1(a) | i) Perform the operation (+12-17) in 2's complement representation. ii) Define each of the following electrical characteristics of logic gates: V_{OH} , V_{IL} , I_{OL} , I_{IH} . | [2+3] 1 | 1 |
| Q.1(b) | i) What is totem pole configuration in TTL circuit? Mention its advantages. ii) Implement the logic function using CMOS, $F = [(A+B)(C+D)(E+F(G+H))]'$. | [2+3] 1 | 2 |
| Q.2(a) | Minimize the following Boolean function using K-Map and further implement using NAND gates: $F(A, B, C, D) = \sum m(0, 4, 5, 6, 8, 9) + d(10, 11, 12, 13, 14, 15)$ | [5] 2 | 2 |
| Q.2(b) | Design the parity bit generator circuit using necessary steps and logic diagram. | [5] 2 | 3 |
| Q.3(a) | Design a BCD-adder circuit following the necessary steps, find the logic expression for BCD-carry and draw the logic diagram. | [5] 3 | 2 |
| Q.3(b) | What is decoder? Design a 4:16 decoder circuit using 3:8 decoders and explain the operation. | [5] 3 | 3 |
| Q.4(a) | (i) What is D-flip-flop? Draw the circuit for it. (ii) What is shift register? Explain the working of a serial-in-parallel out shift register (4-bit) with necessary inputs and outputs and circuit diagram. | [2+3] 4 | 2 |
| Q.4(b) | Design a clocked sequential circuit using J-K flip-flop that would go through the following states: $00 \rightarrow 10 \rightarrow 11 \rightarrow 10 \rightarrow 00 \dots$ (Follow the steps as: state table, excitation table, simplification and circuit diagram) | [5] 4 | 3 |
| Q.5(a) | What is programmable logic device? Mention the advantages of it. Explain the working of a PLA with a standard logic circuit and diagram. | [5] 4 | 2 |
| Q.5(b) | Explain the working of an astable multivibrator using any technique and mention the equation for time-period of the output square wave. Write the expression of duty cycle of the output signal. | [5] 5 | 3 |

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