BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: B.TECH. **SEMESTER : V**
BRANCH: AIML **SESSION : MO/2024**

SUBJECT: CS239 OPERATING SYSTEM

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Specify elements of a process. Explain and illustrate the structure of a process control block with a diagram.	[5]	1	1,2
Q.1(b)	Illustrate the distinction between threads and processes from the point of view of process management with a diagram.	[5]	2	
Q.2(a)	Why is scheduling a matter of managing queues? Explain the queuing diagram for scheduling of processes.	[5]	2	2
Q.2(b)	Consider the following scenario of processes with their priority: Draw a Gantt chart for the execution of processes, showing their start time and end time, using priority-number based scheduling. Calculate turnaround time, normalized turnaround time, and waiting time for each process, and average turnaround time, average normalized turnaround time, and average waiting time for the system.	[5]	2	3

Process	Arrival Time	Execution Time	Priority
P_1	0	3	3
P_2	2	7	4
P_3	3	5	1
P_4	5	9	2

Q.3(a)	Specify the requirements of any facility to provide support for mutual exclusion. Briefly explain different hardware approaches to mutual exclusion.	[5]	3	1,2
Q.3(b)	Explain principles and characteristics of deadlock with resource allocation graph.	[5]	3	2,3
Q.4(a)	Differentiate distinct memory management techniques with their strengths and weaknesses.	[5]	4	4
Q.4(b)	Specify the steps for logical to physical address translation. For a system with 16-bit addresses, 1K page size and 10 bits offset field, translate the logical address for address value $(1502)_{10}$ to its corresponding physical address.	[5]	5	3
Q.5(a)	Explain different layers of I/O organization with diagrams.	[5]	4	2
Q.5(b)	Briefly explain different disk scheduling algorithms.	[5]	4	2

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