BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: B.Sc MLT **SEMESTER: III**
BRANCH: MLT **SESSION: MO/2024**

SUBJECT: BMT305 DIGITAL ELECTRONICS SYSTEM

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Explain the working of special gates with circuit symbol, truth table and timing diagrams.	[5]	1	2
Q.1(b)	Implement NOT, AND, OR and NAND gates by using only NOR gates.	[5]	1	3
Q.2(a)	Enlighten the basics of SOP and POS with examples. Also discuss the importance of Veitch diagram.	[5]	2	2
Q.2(b)	Reduce the function using K-map technique and implement it using NAND gates. f (P, Q, R, S) = $\sum m$ (0, 7, 8, 9, 10, 12) + d (2, 5, 13).	[5]	2	3
Q.3(a)	Explain the working principle of Transistor Transistor Logic (TTL). Also write the silent features for it.	[5]	3	2
Q.3(b)	Draw and explain the working principle of CMOS. Also Write its advantages and disadvantages.	[5]	3	3
Q.4(a)	Draw and explain the full adder circuit and implement it using gates.	[5]	4	2
Q.4(b)	Discuss the working principle of multiplexer. Implement OR and NAND gates using MUX.	[5]	4	3
Q.5(a)	Differentiate between Latch and Flip flop. Explain the truth table of J K flip flop.	[5]	5	2
Q.5(b)	Explain the circuit diagram for serial input and serial output (SISO) shift register.	[5]	5	3

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