BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2023)

CLASS: B. Tech. **SEMESTER : VII**
BRANCH: EEE **SESSION : MO/2023**

SUBJECT: EE423 VSLI SYSTEMS

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Draw the transistor level circuit diagram of an inverter and implement the same in Verilog HDL using switch level modeling style.	[2]	CO1,CO2	L3
Q.1(b)	Draw the Y chart. Explain the different design domains.	[3]	CO1,CO2	L1
Q.2(a)	Draw the transistor level circuit diagram of carry out function Co=A.B + Ci (B+A), where Ci is the input carry to a 1-bit full adder.	[2]	CO1,CO2	L2
Q.2(b)	Provide the circuit level specification(SPICE deck) of carry out function Co=A.B + Ci (B+A), where Ci is the input carry to a 1-bit full adder.	[3]	CO1,CO2	L3
Q.3(a)	What are the advantages of SOI CMOS process?	[2]	CO1,CO2	L1
Q.3(b)	Draw the circuit diagram and write the Verilog code for sum and carry function of full adder.	[3]	CO1,CO2	L3
Q.4(a)	What are the common materials used as masks for CMOS technologies?	[2]	CO1,CO2	L1
Q.4(b)	Compute the sheet resistance of a 0.22um thick copper wire in a 65nm process. Find the total resistance if the wire is 0.125um wide and 1mm long. For copper, $\rho = 2.2\ \mu\Omega$-cm.	[3]	CO1,CO2	L2
Q.5(a)	What is (i) ion implantation (ii) diffusion?	[2]	CO1,CO2	L1
Q.5(b)	What is latchup? Explain with the help of diagram. How it can be prevented?	[3]	CO1,CO2	L2

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