BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/2023**

SUBJECT: EC427 ASIC DESIGN

TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Write short note on history of VHDL.	[5]	1	1
Q.1(b)	Explain the various building blocks of VHDL.	[5]	2	1
Q.2(a)	Explain the process statement with the help of example. Differentiate between signal and variable assignment.	[5]	1	1
Q.2(b)	Write the VHDL code for half adder and full adder.	[5]	2	2
Q.3(a)	Write note on data types and objects.	[5]	1	1
Q.3(b)	Explain associate lists and interface lists. Also explain conversion function and resolution function.	[5]	1	1
Q.4(a)	Explain packages and package declaration.	[5]	2	1
Q.4(b)	Explain deferred constants and subprogram declaration.	[5]	2	1
Q.5(a)	Write VHDL code for priority encoder.	[5]	2	2
Q.5(b)	Write VHDL code for binary to gray and gray to binary decoders.	[5]	2	2

:::::24/11/2023 M:::::