**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**
**(MID SEMESTER EXAMINATION MO/2023)**

**CLASS: B. Tech.** **SEMESTER : VII**
**BRANCH: ECE** **SESSION : MO/2023**

**SUBJECT: EC427 ASIC DESIGN**

**TIME: 02 Hours** **FULL MARKS: 25**

**INSTRUCTIONS:**
**1. The question paper contains 5 questions each of 5 marks and total 25 marks.**
**2. Attempt all questions.**
**3. The missing data, if any, may be assumed suitably.**
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

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| Q.1(a) | Explain the basic building blocks of VHDL. | [2] | CO1,CO2 | L1 |
| Q.1(b) | Write VHDL code for 2X1 MUX. | [3] | CO1,CO2 | L3 |
| Q.2(a) | Write a brief note on history of VHDL. | [2] | CO1,CO2 | L1 |
| Q.2(b) | Write the VHDL code for full adder circuit using structural style of modeling. | [3] | CO1,CO2 | L3 |
| Q.3(a) | What are different types of architecture in VHDL? Explain with the help of examples. | [2] | CO1,CO2 | L4 |
| Q.3(b) | Write VHDL code for gray to binary converter. | [3] | CO1,CO2 | L3 |
| Q.4(a) | Differentiate between sequential and concurrent assignment statements. | [2] | CO1,CO2 | L4 |
| Q.4(b) | Explain process statement with the help of example. | [3] | CO1,CO2 | L2 |
| Q.5(a) | Explain the following with respect to VHDL:<br>(i) Driver (ii) Bus | [2] | CO1,CO2 | L2 |
| Q.5(b) | Write the syntax for FOR loop and WHILE loop. | [3] | CO1,CO2 | L3 |

**:::::22/09/2023 M:::::**