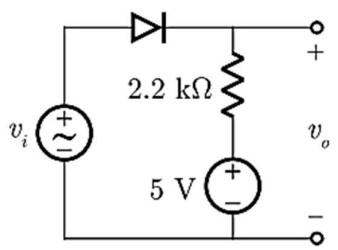
BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION MO/2023)

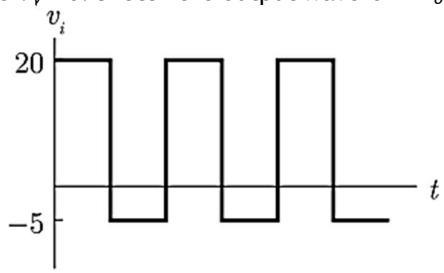
CLASS: B.TECH. **SEMESTER: I**
BRANCH: CSE/AIML/ECE/EEE **SESSION: MO/2023**

SUBJECT: EC101 BASICS OF ELECTRONICS AND COMMUNICATION ENGINEERING
TIME: 02 Hours **FULL MARKS: 25**

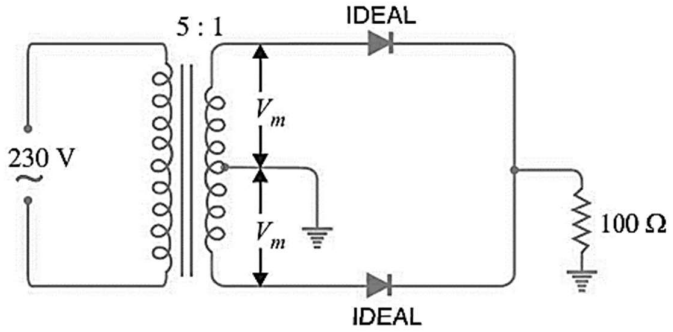
INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

		Mark	CO	BL
Q.1(a)	The reverse saturation current of a germanium diode operated at 300 Kelvin is 10μA. Estimate its value at 350 Kelvin. Schematize the volt-ampere characteristic of an ideal p-n diode.	[2]	1	2,6
Q.1(b)	Write down the equation that gives volt-ampere relationship of diode. It contains the temperature implicitly in the two symbols. Write down what are those? Briefly explain why diode current depends on temperature.	[3]	1	2,3
Q.2(a)	A Ge diode is operated at a junction temperature of 27℃. For a forward current of 10 mA, V_D is found to be 0.3 V. (a) If V_D = 0.4 V, calculate the forward current. (b) Calculate the reverse saturation current.	[2]	1	4
Q.2(b)	Schematize the V-I characteristic of a Zener diode. Sketch the circuit diagram in which such a diode is used to regulate the voltage across load resistance R_L against changes due to variations in load current and supply voltage. Briefly explain its operation to do so.	[3]	1	3,6
Q.3(a)	Consider the given circuit and a waveform for the input voltage v_i as shown in figure below. The diode in circuit has cut in voltage V_γ = 0. Sketch the output waveform v_o.	[2]	1	3





Q.3(b)	In the center-tap circuit shown in Figure, the diodes are assumed to be ideal i.e., having zero internal resistance. Calculate (i) d.c. output voltage, (ii) peak inverse voltage, (iii) rectification efficiency.	[3]	1	4



PTO

Q.4(a)	Briefly explain whether the input circuit [i.e., base-emitter junction (J_E)], and output circuit [i.e., base-collector junction (J_C)] offer the same level (value) of resistance or not. If not, why. Why are NPN and PNP devices called transistors?	[2]	2	2
Q.4(b)	Sketch the structure of a PNP transistor and write down its terminal currents and internal currents with appropriate direction when it is properly biased. Briefly explain the reason for the flow of such currents.	[3]	2	3
Q.5(a)	Schematize the basic structure (simplified view) of an n-channel junction field-effect transistor (JFET) and label its terminals. Sketch its I_D—V_{DS} characteristics.	[2]	2	1,3,6
Q.5(b)	Demonstrate the types of MOSFETs (based on normally ON/OFF trait) by drawing their structures. Label all the regions and terminals of the same.	[3]	2	1,2

:::::18/10/2023:::::